United States District Court,
E.D. Texas, Marshall Division.

OPTI Inc,
Plaintiff.
v.
ADVANCED MICRO DEVICES, INC,
Defendant.

Civil Action No. 2:06-CV-00477 CE

July 17, 2008.

CLAIM CONSTRUCTION ORDER

CHARLES EVERINGHAM IV, United States Magistrate Judge.

This case came before the Court on July 9, 2008 for hearing on all claim construction issues pursuant to the Docket Control Order of November 21, 2007. The Court has reviewed the briefs of the parties and the argument had in open Court. Having carefully considered the parties' positions, the language of the claims in light of the specification and the pertinent portions of the prosecution history, and having evaluated the disputed claim terms in light of the principles of claim construction announced by the Federal Circuit in Phillips v. AWH Corp., 415 F.3d 1303 (Fed.Cir .2005) (*en banc*) and other cases, the Court rules as set forth below as to the claim terms in dispute and enters as its order the claim constructions agreed to by the parties.

U.S. Patent 5,710,906 Claim 1	**Term/Element for Construction**	**Court's Construction**	**Agreed Construction**
[1.1] A method for transferring a plurality of data units between a **bus master** and a respective plurality of memory locations at sequential memory location addresses in an address space of a secondary memory, for use with a host processing unit and a first cache memory which caches memory locations of said secondary memory for said host processing unit, said first cache memory having a line size of L bytes, comprising the steps of:	"**first cache memory**"	[AGREED]	the first level of cache memory, commonly referred to as L1 cache memory.
	"**said first cache memory**"	[AGREED]	*See* "first cache memory"
	"**secondary memory**"	[AGREED]	memory located logically behind the first level cache

			memory, i.e., DRAM memory and, if present, L2 and L3 cache memory.
	"**bus master**"	an I/O-bus device that initiates a data transfer on the I/O bus.	
[1.2] Sequentially transferring data units between **said bus master** and said secondary memory beginning at a starting memory location address in said secondary memory address space and continuing beyond an L-byte boundary of said secondary memory address space, said sequentially transferred data units including a last data unit before said L-byte boundary and a first data unit beyond said L-byte boundary; and	"**Sequentially transferring data units between said bus master and said secondary memory**"	[AGREED]	moving data units between the bus master and the secondary memory in the sequence in which they are stored.
	"**said bus master**"	*See* "bus master." Limitation 1.1	
[1.3] **initiating a next-line inquiry, prior to completion of the transfer of the last data unit before said L-byte boundary,** to determine whether an N1'th L-byte line of said secondary memory is cached in a modified state in said first cache memory, said N1'th L-byte line being a line of said secondary memory which includes said first data unit beyond said L-byte boundary.	"**next line**"	[AGREED]	the next sequential cache line.
	"**initiating a next-line inquiry ... to determine whether an N1'th L-byte line of said secondary memory is cached in a modified state in said first cache memory**"	[AGREED]	initiating a next-line inquiry to determine whether the N1th line of data in the first cache memory is different from the corresponding data in the secondary memory.
	"**inquiry**"	an operation for determining whether a line of data in the first cache memory is different from the corresponding data in the	

		secondary memory.	
	"**initiating a next-line inquiry**"	sending a command to perform a next-line inquiry.	
	"**prior to completion of the transfer of the last data unit before said L-byte boundary**"	[AGREED]	prior to completion of the transfer of the last data unit before said L-byte boundary.

U.S. Patent 5,710,906 Claim 7	**Term/Element for Construction**	**Court's Construction**	**Agreed Construction**
[7.1] A method according to claim 1, wherein said **bus master** is a PCI bus master, wherein said first cache memory includes an instruction cache and a data cache, and wherein said host processing unit and said first cache memory are fabricated on a single CPU chip .	"**said first cache memory**"	[AGREED]	*See* Limitation 1.1.
	"**bus master**"	*See* "bus master" Limitation 1.1.	

U.S. Patent 5,710,906 Claim 8	**Term/Element for Construction**	**Court's Construction**	**Agreed Construction**
[8.1] A method according to claim 1, wherein said next-line **inquiry** takes place concurrently with at least one of the data unit transfers in said step of sequentially transferring.	"**concurrently with at least one of the data unit transfers in said step of sequentially transferring**"	[AGREED]	while at least one of the data units is moving from the secondary memory to the bus master.
	"**said step of sequentially transferring**"	[AGREED]	*See* Limitation 1.2 "sequentially transferring data units between said bus master and said secondary memory"
	"**next-line**"	[AGREED]	*See* "next-line" Limitation 1.3
	"**inquiry**"	*See* "inquiry" Limitation 1.3.	

U.S. Patent 5,710,906 Claim 1	**Term/Element for Construction**	**Court's Construction**	**Agreed Construction**
[9.1] A method for transferring data between a **bus**	"**first cache**	[AGREED]	*See* Limitation 1.1

master and a plurality of memory locations at respective addresses in an address space of a secondary memory, for use with a host processing unit and a first cache memory which caches memory locations of said secondary memory for said host processing unit, said first cache memory having a line size of L bytes, comprising the steps of:	**memory**"		
	"**said first cache memory**"	[AGREED]	*See* Limitation 1.1
	"**secondary memory**"	[AGREED]	*See* Limitation 1.1
	"**bus master**"	*See* Limitation 1.1.	
[9.2] sequentially transferring at least three data units between **said bus master** and said secondary memory beginning at a first starting memory location address in said secondary memory address space and continuing sequentially beyond an L-byte boundary of said secondary memory address space; and	" **sequentially transferring at least three data units between said bus master and said secondary memory**"	[AGREED]	moving at least three data units between the bus master and the secondary memory in the sequence in which they are stored.
	"**said bus master**"	*See* Limitation 1.1.	
[9.3] **prior to completion of the transfer of the first data unit beyond said L-byte boundary, determining whether an N1'th L-byte line of said secondary memory is cached in a modified state in said first cache memory,** said N1'th L-byte line being the line of said secondary memory which includes said first data unit beyond said L-byte boundary,	"**prior to the completion of the transfer of the first data unit beyond said L-byte boundary**"	[AGREED]	prior to completion of the transfer of the first data unit beyond said L-byte boundary.
	"**determining whether an N1'th L-byte line of said secondary memory is cached in a modified state in said first cache memory**"	*See* Limitation 1.3 "initiating a next-line inquiry ... to determine whether ..."	
[9.4] all of said transfers of data units in said step of sequentially transferring, occurring at a **constant rate.**	"**said transfers of data units in said step of sequentially transferring**"	[AGREED]	*See* Limitation 9.2 "sequentially transferring at least three data units between said bus master and

			said secondary memory."
	"**constant rate**"	A uniform rate.	

U.S. Patent 6,405,291 Claim 73	**Term/Element for Construction**	**Court's Construction**	**Agreed Construction**
[73.1] A method for transferring a plurality of data units to a **bus master** from a respective plurality of memory locations at sequential memory location addresses in an address space of a secondary memory, for use with a host processing unit and a cache memory which caches memory locations of said secondary memory for said host processing unit, said cache memory having a line size of L bytes, and each data unit having a size equal to the largest size that can be transferred to **said bus master** in parallel, comprising the steps of:	"**cache memory**"	[AGREED]	high-speed memory that stores copies of portions of main memory data. The cache memory is organized into multiple lines, each having a size of L-bytes.
	"**secondary memory**"	[AGREED]	*See* '906 Patent, Limitation 1.1
	"**bus master**"	*See* '906 Patent, Limitation 1.1.	
	"**said bus master**"	*See* '906 Patent, Limitation 1.1.	
[73.2] sequentially transferring data units to **said bus master** from said secondary memory according to a PCI-bus burst transaction, beginning at a starting memory location address in said secondary memory address space and continuing beyond at least first and second L-byte boundaries of said secondary memory address space, each L-byte line of said transaction requiring at least 8 data unit transfers to said bus master; and	"**sequentially transferring data units to said bus master from said secondary memory**"	[AGREED]	moving data units to the bus master from the secondary memory in the sequence in which they are stored
	"**said bus master**"	*See* '906 Patent, Limitation 1.1.	
[73.3] during the transfer of the data units for each entire N'th L-byte line in said step of transferring, **initiating one and only one snoop access** of said cache memory, said snoop	"**during the transfer of the data units for**	[AGREED]	while the data units for each entire N'th L-

accesses each specifying the respective N1'th L-byte line and being initiated early enough such that they can be sampled by said host processing unit prior to completion of the transfer to said bus master of the last data unit in the respective N'th L-byte line,	**each entire N'th L-byte line**"		byte line are moving to the bus master from the secondary memory
	"**the transfer of the data units**"	[AGREED]	*See* Limitation 73.2 "sequentially transferring data units to said bus master from said secondary memory."
	"**said cache memory**"	[AGREED]	*See* Limitation 73.1.
	"**N1'th L-byte line**"	[AGREED]	the next sequential line following line N
	"**initiating one and only one snoop access**"	[AGREED]	initiating one and only one next-line inquiry. *See* '906 Patent 1.3 ("initiating a next-line inquiry ...").
[73.4] wherein said step of transferring comprises the step of transferring to said bus master three sequential data units including the last data unit before said first L-byte boundary and the first data unit beyond said first L-byte line, all at a **constant rate,**	"**said step of transferring**"	[AGREED]	*See* Limitation 73.2 "sequentially transferring data units to said bus master from said secondary memory."
	"**constant rate**"	*See* '906 Patent, Limitation 9.4.	
[73.5] and wherein said step of transferring further	"**said step of**	[AGREED]	*See*

comprises the step of transferring to said bus master three sequential data units including the last data unit before said second L-byte boundary and the first data unit beyond said second L-byte line, all at a constant rate.	**transferring**"		Limitation 73.2 "sequentially transferring data units to said bus master from said secondary memory."

U.S. Patent 6,405,291 Claim 74	**Term/Element for Construction**	**Court's Construction**	**Agreed Construction**
[74.1] A method according to claim 73, wherein said step of sequentially transferring data units continues further beyond a third L-byte boundary of said secondary memory, and wherein said step of transferring further comprises the step of transferring three sequential data units including the last data unit before said third L-byte boundary and the first data unit beyond said third L-byte line, all at a **constant rate.**	"**said step of sequentially transferring data units**"	[AGREED]	*See* Limitation 73.2 "sequentially transferring data units to said bus master from said secondary memory."
	"**said step of transferring**"	[AGREED]	*See* Limitation 73. 2 "sequentially transferring data units to said bus master from said secondary memory."
	"**constant rate**"	*See* '906 Patent, Limitation 9.4.	

U.S. Patent 6,405,291 Claim 88	**Term/Element for Construction**	**Court's Construction**	**Agreed Construction**
[88.1] **Controller apparatus** for a computer system which includes a secondary memory having an address space, a **bus master,** a host processing unit and a cache memory which caches memory locations of said secondary	"**cache memory**"	[AGREED]	*See* Limitation 73.1

memory for said host processing unit, said cache memory having a line size of L bytes, and each data unit having a size equal to the largest size that can be transferred to **said bus master** in parallel, said controller apparatus comprising circuitry which in a mode of operation, in response to a PCI-bus burst read transaction initiated by said bus master,			
	"**secondary memory**"	[AGREED]	*See* '906 Patent, Limitation 1.1
	"**said cache memory**"	[AGREED]	*See* Limitation 73.1
	"**bus master**"	*See* '906 Patent, Limitation 1.1.	
	"**said bus master**"	See '906 Patent, Limitation 1.1.	
[88.2] **sequentially transfers data units to said bus master from said secondary memory according to said PCI-bus burst transaction, beginning at a starting memory location address in said secondary memory address space and continuing beyond at least first, second and third L-byte boundaries of said secondary memory address space, each full L-byte line of said transaction requiring at least 8 data unit transfers to said bus master, a plurality of sequential data units bracketing at least said first, second and third L-byte boundaries being transferred to said bus master at a constant rate, said constant rate being dependent upon the frequency of a PCI-bus clock provided to said bus master;** and	"**sequentially transfers data units to said bus master from said secondary memory**"	[AGREED]	moving data units to the bus master from the secondary memory in the sequence in which they are stored
	"**constant rate**"	*See* '906 Patent,	

		Limitation 9.4	
	"**sequentially transfers data units to said bus master from said secondary memory according to said PCI-bus burst transaction, beginning at a starting memory location address in said secondary memory address space and continuing beyond at least first, second and third L-byte boundaries of said secondary memory address space, each full L-byte line of said transaction requiring at least 8 data unit transfers to said bus master, a plurality of sequential data units bracketing at least said first, second and third L-byte boundaries being transferred to said bus master at a constant rate, said constant rate being dependent upon the frequency of a PCI-bus clock provided to said bus master**"	This is not a means-plus-function element and, therefore, it need not be construed according to 35 U.S.C. s. 112 para. 6.	
[88.3] **during the transfer of the data units for each entire N'th L-byte line according to said transaction, initiates one and only one snoop access of said cache memory, said snoop access specifying the respective N1'th L-byte line and being initiated early enough such that it can be sampled by said host processing unit prior to completion of the transfer to said bus master of the last data unit in the respective N'th L-byte line, said snoop accesses being sampled by said host processing unit in accordance with a host clock signal having a frequency that is at least twice said PCI-bus clock frequency.**	"**during the transfer of the data units for each entire N'th L-byte line**"	[AGREED]	*See* Limitation 73.3 "during the transfer of the data units for each entire N'th L-byte line."
	"**N1'th L-byte line**"	[AGREED]	the next sequential line following line N.
	"**initiates one and only one snoop access**"	*See* Limitation 73.3	

	"**during the transfer of the data units for each entire N'th L-byte line according to said transaction, initiates one and only one snoop access of said cache memory, said snoop access specifying the respective N1'th L-byte line and being initiated early enough such that it can be sampled by said host processing unit prior to completion of the transfer to said bus master of the last data unit in the respective N'th L-byte line, said snoop accesses being sampled by said host processing unit in accordance with a host clock signal having a frequency that is at least twice said PCI-bus clock frequency**"	This is not a means-plus-function element and, therefore, it need not be construed according to 35 U.S.C. s. 112 para. 6.	

U.S. Patent 6,405,291 Claim 89	**Term/Element for Construction**	**Court's Construction**	**Agreed Construction**
89. Apparatus according to claim 88, wherein said circuitry further **reads data from said secondary memory at a constant rate for said plurality of sequential data units bracketing at least said first, second and third L-byte boundaries.**	"**constant rate**"	*See* '906 Patent, Limitation 9.4	
	"**reads data from said secondary memory at a constant rate for said plurality of sequential data units bracketing at least said first, second and third L-byte boundaries**"	This is not a means-plus-function element and, therefore, it need not be construed according to 35 U.S.C. s. 112 para. 6.	

E.D.Tex.,2008.
Opti Inc. v. Advanced Micro Devices, Inc.