United States District Court,
N.D. California.

SYNOPSYS, INC,
Plaintiff.
v.
MAGMA DESIGN AUTOMATION, INC,
Defendant.

No. C-04-3923 MMC

Aug. 23, 2005.

AMENDED ORDER RE: CLAIM CONSTRUCTION OF UNITED STATES PATENTS NOS. 6,453,446, 6,725,438**, AND** 6,378,114

MAXINE M. CHESNEY**, District Judge.**

Before the Court is the parties' dispute over the proper construction of United States Patents Nos. 6,453,446 ('the '446 patent"), 6,725,438 ("the '438 patent"), and 6,378,114 ("the '114 patent").

BACKGROUND

Synopsys alleges that Magma infringes three patents: the '446 patent, titled "Timing Closure Methodology"; the '438 patent, which also is titled "Timing Closure Methodology," and the '114 patent, titled "Method for the Physical Placement of an Integrated Circuit Adaptive to Netlist Changes." (*See* Second Amended Complaint ("SAC") para.para. 92-102.) In the '446 and '438 patents, Lukas van Ginneken ("van Ginneken") is identified as the sole inventor, and in the '114 patent, van Ginneken is identified as a co-inventor. (*See* id. Exs. H, I, and J at 1.) The '446 and '438 patents identify Magma as the assignee. (*See* id. Exs. H and I at 1.) The '114 patent identifies Synopsys as the assignee. (*See* id. Ex. J at 1.) Synopsys alleges that it is the rightful owner of all three patents as a result of a Proprietary Information and Inventions Agreement ("Agreement") that van Ginneken, a former employee of Synopsys, entered into with Synopsys on May 17, 1995. (*See* id. para. para. 10-18, 96-97.)

LEGAL STANDARD

The construction of a patent claim is a matter of law for the court. *See* Markman v. Westview Instruments, Inc., 517 U.S. 370, 372 (1996). As the claim language defines the scope of the claim, the claim construction analysis always begins with the words of the claim. *See* Teleflex, Inc. v. Ficosa North America Corp., 299 F.3d 1313, 1324 (Fed.Cir.2002). The words of a claim are "generally given their ordinary and customary meaning," and the "ordinary and customary meaning of a claim term is the meaning that the term would have to a person of ordinary skill in the art in question at the time of the invention, i.e., as of the effective filing date of the patent application." *See* Phillips v. AWH Corp ., 2005 WL 1620331 at (Fed.Cir. July 12, 2005). "[T]he person of ordinary skill in the art is deemed to read the claim term not only in the context of

the particular claim in which the disputed term appears, but in the context of the entire patent, including the specification."

"Because the meaning of a claim term as understood by persons of skill in the art is often not immediately apparent, and because patentees frequently use terms idiosyncratically, the court looks to those sources available to the public that show what a person of skill in the art would have understood disputed claim language to mean," including "the words of the claims themselves, the remainder of the specification, the prosecution history, and extrinsic evidence concerning relevant scientific principles, the meaning of technical terms, and the state of the art." *See id*. at *6. "[T]he context in which a term is used in the asserted claim can be highly instructive." *Id*. In addition, "[b]ecause the claim terms are normally used consistently throughout the patent, the usage of a term in one claim can often illuminate the meaning of the same term in other claims." *See id* . at *7.

The claims must be read in view of the specification, which is required to "describe the manner and process of making and using" the patented invention in "full, clear, concise, and exact terms." *See id*. at *7, *8. "[T]he specification may reveal a special definition given to a claim term by the patentee that differs from the meaning it would otherwise possess," in which case "the inventor's lexicography governs." *See id*. at *8. "In other cases, the specification may reveal an intentional disclaimer, or disavowal, of claim scope by the inventor," in which case "the inventor's intention, as expressed in the specification, is dispositive." *See id*.

"Like the specification, the prosecution history provides evidence of how the PTO and the inventor understood the patent." *Id*. at *9. The prosecution history "often lacks the clarity of the specification and thus is less useful for claim construction purposes," however, because it "represents an ongoing negotiation between the PTO and the applicant, rather than the final product of the negotiations." *See id*. "Nonetheless, the prosecution history can often inform the meaning of the claim language by demonstrating how the inventor understood the invention and whether the inventor limited the invention in the course of prosecution, making the claim scope narrower than it would otherwise be." *Id*.

In construing the claims of a patent, courts also may consult extrinsic evidence, including "expert and inventor testimony, dictionaries and learned treatises." *See id*. at *10. "While extrinsic evidence can shed useful light on the relevant art," it is "less significant than the intrinsic record in determining the legally operative meaning of claim language." *See id*. Technical dictionaries may help a court "to better understand the underlying technology and the way in which one of skill in the art might use the claim terms." *Id*. In addition, "expert testimony can be useful to a court for a variety of purposes, such as to provide background on the technology at issue, to explain how an invention works, to ensure that the court's understanding of the technical aspects of the patent is consistent with that of a person of skill in the art, or to establish that a particular term in the patent or the prior art has a particular meaning in the pertinent field." *Id*. Courts should disregard conclusory testimony by experts, however, as well as any expert testimony that is "clearly at odds with the claim construction mandated by the claims themselves, the written description, and the prosecution history [.]" *See id*. "In sum, extrinsic evidence may be useful to the court, but it is unlikely to result in a reliable interpretation of patent claim scope unless considered in the context of the intrinsic evidence," i.e., the claim language, specification, and prosecution history. *See id*. at *11.

An accused infringer may overcome the heavy presumption that a claim term carries its ordinary and customary meaning, "but he cannot do so simply by pointing to the preferred embodiment or other structures or steps disclosed in the specification or prosecution history." *See* CCS Fitness v. Brunswick Corp., 288 F.3d 1359, 1366 (Fed.Cir.2002). "Though understanding the claim language may be aided by the explanations

contained in the written description, it is important not to import into a claim limitations that are not a part of a claim." SuperGuide Corp. v. DirecTV Enterprises, Inc., 358 F.3d 870, 875 (Fed.Cir.2004.) "For example, a particular embodiment appearing in the written description may not be read into a claim when the claim language is broader than the embodiment." *Id*.

DISCUSSION

The parties dispute the proper claim construction of certain terms used in the claims of the patents at issue. FN1 The Court begins its analysis with the '446 and ' 438 patents. FN2

FN1. Although the '446 and '438 patents were assigned by the inventor to Magma, Magma argues herein for a narrow construction of the disputed claim language, while Synopsys argues for a broader construction.

FN2. The '446 and '438 patents derive from the same patent application and share the same specification. For ease of reference, when citing to the shared specification of the '446 and '438 patents, the Court will cite only to the '446 patent.

A. The '446 and '438 Patents

The '446 and '438 patents are both titled "Timing Closure Methodology." The inventions set forth in the '446 and '438 patents "relate generally to the field of integrated circuit design and more specifically to a methodology for meeting timing constraints in the design of digital circuits." (*See* '446 patent at 1:29-31.) The basic building blocks of integrated circuits ("IC") are called "gates" (or "cells"), which are interconnected with each other by wires. (*See* Harris Decl. para. 15; *see also* Sechen Decl. para. 19.) Each path between two gates or cells has an associated "delay," which is the amount of time it takes for data to pass from one end of the path to the other. (*See* Harris Decl. para. 23; *see also* Sechen Decl. para. 22.) The delay results from certain electronic characteristics of the gates and wires, primarily capacitance (or "load"). (*See* Harris Decl. para. 23; *see also* Sechen Decl. para. 22.) A gate must have a certain "driving capability" to drive the load "defined by the wires and gates connected to its input"; if the gate must drive a longer wire (i.e., a longer load) without incurring additional delay, it must have an increased driving capability. (*See* Harris Decl. para. 23; *see also* Sechen Decl. para. 23.)

The process of IC design involves logic synthesis and physical design. (*See* Harris Decl. para. 16.) Logic synthesis "refers to the conversion of a high-level circuit description ... into a more detailed electronic circuit description such as a 'netlist,' which is a list of cells, their interconnections, and other information." (*See* id. para. 17.) "Physical design refers to the process of placing and routing gates on an IC to create a 'layout,' which is a detailed blueprint describing the actual physical dimensions of the circuit elements (e.g., gates and wires) to be formed on the chip." (*See* id. para. 18.) The placement step includes determining physical locations on the chip for all cells in the netlist; the routing step includes determining the routes of the wires connecting the cells. (*See* id. para.para. 18-19; *see also* Sechen Decl. para.para. 18-20.) The goal of IC designers is to design an IC that is "small, yet powerful and fast." (*See* Harris Decl. para. 20.)

In the conventional IC design process, the size of each cell is chosen at the outset and remains constant once chosen. (*See* '446 patent at 1:20-34.) During placement, the "net (wire) lengths of the circuit are estimated," but said lengths are difficult to estimate accurately. (*See* id. at 1:26-27, 1:34-36.) Under the conventional process, "[t]his difficulty in accurately predicting net lengths leads to unpredictable delay effects after cell

placement occurs." (*See* id. at 1:41-42.) "For example, some nets turn out to be longer in length than expected." (Id. at 1:42-44.) "These longer nets cause longer delays which prevent satisfaction of timing constraints in the digital circuit." (Id. at 1:44-46.) "Thus, under the conventional design approach, timing closure [i.e., satisfaction of timing constraints] is not certain until after placement." (Id. at 1:46-47.) "Failure to achieve timing closure after placement leads to additional expenses and other problems for the designer." (Id. at 1:48-49.)

The inventions set forth in the '446 and '438 patents are designed to overcome this deficiency in the conventional process. (*See* id. at 3:11-14.) In general terms, the invention abandons the conventional technique of beginning the design process with cells of fixed sizes, and instead begins the design process by using delays to determine the size and placement of cells. (*See, e.g.,* id., Abstract and 3:16-41.)

1. "Step Plus Function"

As an initial matter, the parties dispute whether subsection (a) of claim 1 of the '446 patent is a "step-plus-function" claim subject to 35 U.S.C. s. 112, para. 6, which provides:

An element in a claim for a combination may be expressed as a means or a step for performing a specified function without the recital of structure, material, or acts in support thereof, and such claim shall be construed to cover the corresponding structure, material, or acts described in the specification and equivalents thereof.

35 U.S.C. s. 112, para. 6. Under this provision, an inventor "can describe an element of his invention by the result accomplished or the function served, rather than describing the item or element to be used (e.g., 'a means of connecting Part A to Part B,' rather than 'a two-penny nail')." *See* Warner-Jenkinson Co., Inc. v. Hilton Davis Chemical Co., 520 U.S. 17, 27 (1997).

The statute "can apply not only to a combination of mechanical elements, but also to 'a combination of ... steps in a process claim.' " *See* Masco Corp. v. United States, 303 F.3d 1316, 1326 (Fed.Cir.2002). The Federal Circuit has held that the statute permits "an element in a combination method or process claim [to] be recited as a step for performing a specified function without the recital of acts in support of the function." *See* O.I. Corp. v. Tekmar Co. Inc., 115 F.3d 1576, 1583 (Fed.Cir.1997). "The price that must be paid for use of that convenience," however, is that "such a claim covers only the specific acts recited in the specification for performing that function, and equivalent acts." *See id.; see also* Seal-Flex, Inc. v. Athletic Track and Court Construction, 172 F.3d 836, 850 (Fed.Cir.1999) (Rader, J., concurring).

There is a presumption that the claims are in step-plus-function format when the drafter uses the term "steps for." *See* Masco, 303 F.3d at 1326. By contrast, where the claim employs the term "steps of," there is no presumption that the claims are in step-plus-function format, *see* id. at 1327, because "[m]ethod claims necessarily recite the steps of the method, and the preamble words that 'the method comprises the steps of' do not automatically convert each ensuing step into the form of s. 112 para. 6." *See* Cardiac Pacemakers, Inc. v. St. Jude Medical, Inc., 381 F.3d 1371, 1382 (Fed.Cir.2004). "[W]here a method claim does not contain the term 'step[s] for,' a limitation of that claim cannot be construed as a step-plus-function limitation without a showing that the limitation contains no act." *See* Masco, 303 F.3d at 1327. FN3

FN3. "[T]he 'underlying function' of a method claim element corresponds to *what* that element ultimately accomplishes in relationship to what the other elements of the claim and the claim as a whole accomplish.

'Acts,' on the other hand, correspond to *how* the function is accomplished." *See* Masco, 303 F.3d at 1327 (quoting Seal-Flex, 172 F.3d at 849-50 (Rader, J., concurring) (emphasis in original)); *see also* O.I. Corp., 115 F.3d at 1583-84 ("We interpret the term 'steps' to refer to the generic description of elements of a process, and the term 'acts' to refer to the implementation of such steps.").

"[E]ven where the drafter employs the "step for" language," however, " 'section 112, para. 6 is implicated ... only when steps plus function *without acts* are present' " in the claim language. *See* Masco, 303 F.3d at 1326 (quoting O.I. Corp., 115 F.3d at 1582) (ellipses and emphasis in original). If the claim language sets forth an act to perform the desired function, then the claim is not in step-plus-function format. *See id*. at 1327. In addition, "[m]erely claiming a step by itself, or a series of steps, without recital of a function does not trigger the application of s. 112, paragraph 6." Epcon Gas Systems, Inc. v. Bauer Compressors, Inc., 279 F.3d 1022, 1028 (Fed.Cir.2002).

"Only a few cases have found the existence of a step-plus-function claim element." *See* Seal-Flex, 172 F.3d at 850 n. 5 (Rader, J., concurring) (citing In re Roberts, 470 F.2d 1399 (CCPA 1973) and *Ex Parte* Zimmerley, 153 U.S.P.Q. 367 (BPA 1966)). In *Roberts,* the claim language at issue provided: "The method of corrugating polyethylene terephthalate film which comprises shaping said film at a temperature in the range of about 100 (deg.) to 175 (deg.) C. by pressing said film between two coacting rotating surfaces and reducing the coefficient of friction of the resulting film to below about 0.40 as determined by the Bell test." *See* Roberts, 470 F.2d at 1400. The Court of Customs and Patent Appeals held that the phrase "reducing the coefficient of friction of the resulting film to below about 0.40" fell within the scope of s. 112 para. 6 (then codified as s. 112 para. 3) because of "the absence in the claim of specific steps which would bring about the desired friction property." *See* id. at 1402-03. In *Zimmerley,* a lengthy process claim set forth a number of steps, including "raising the pH of the resulting pulp to about 5.0 to precipitate dissolved molybdenum trihydroxide, leaving the ferrous iron values in solution." *See* Zimmerley, 153 U.S.P.Q. at 368. The Patent Office Board of Appeals held that this claim language fell within the scope of s. 112 para. 6 (then codified as s. 112 para. 3) and, accordingly, there was no need for the claim to "recite a specific way of raising the pH." *See* id. at 369.

Here, claim 1 of the '446 patent states:

An automated method for designing an initial integrated circuit layout of a digital circuit with a computer, based upon an electronic circuit description and by using a cell library containing cells, comprising the steps of:

(a) selecting a plurality of cells from the cell library that are intended to be coupled to each other with a plurality of wires and that can be used to implement the digital circuit based on the electronic circuit description input to the computer to obtain a selected plurality of cells, at least some of the selected plurality of cells having an initial intended delay associated therewith for ensuring that predetermined timing constraints are met;

(b) determining a placement of the selected plurality of cells and the wires coupled thereto using a sequence of instructions from the computer program; and

(c) determining the area of the some cells, the area of each some cell being determined using the lengths of the wires coupled to each of said some cells such that the initial intended delay of each some cell is realized,

the length of each wire being determined by the placement of the cells coupled to that wire.

('446 patent at 17:14-35.) As noted, the parties dispute whether subsection (a) is stated in step-plus-function format.

Because claim 1 uses the phrase "steps of" rather than "steps for," there is no presumption that subsection (a) is in step-plus-function format. *See* Masco, 303 F.3d at 1326-27. Because the claim "does not contain the term 'step[s] for,' a limitation of that claim cannot be construed as a step-plus-function limitation without a showing that the limitation contains no act." *See* id. at 1327. In subsection (a), the claim specifies the act of "selecting a plurality of cells from the cell library ... at least some of the selected plurality of cells having an initial intended delay associated therewith" as a way of achieving the specified function, in particular, "ensuring that predetermined timing constraints are met." (*See* '446 patent at 17:18-26.) As subsection (a) includes both a function and an act, it is not in step-plus-function format. *See* Masco, 303 F.3d at 1327.

2. Disputes as to specific claim terms

a. Initial intended delay

Disputed Claim Language	Synopsys's Proposed Construction	Magma's Proposed Construction
Initial intended delay	a delay set as a target	delay determined during library analysis that is intended to be maintained constant prior to and after placement/routing

The phrase "initial intended delay" appears in claims 1, 8, 12, 13, 14, 16, 21, 35, 43, 49, and 50 of the '446 patent. (*See* '446 patent at 17:14-35, 1:65-67, 18:14-28, 18:32-35, 18:45-63, 19:51-20:8, 20:37-21:18, 22:1-12.) In claim 1, for example, the phrase appears twice, specifically, in subsection (a), which requires that "at least some of the selected plurality of cells" have "an initial intended delay associated therewith for ensuring that predetermining timing constraints are met," and, thereafter, in subsection (c), which requires "determining the area of the some cells, the area of each some cell being determined using the lengths of the wires coupled to each of said some cells such that the initial intended delay of each some cell is realized [.]" (*See* id. at 17:23-25, 17:30-33.) The key disputes between the parties concern (1) when the "initial intended delay" is selected, and (2) whether the "initial intended delay" must remain constant once selected, or whether the selected delay may be modified at some point in the process.

The phrase "initial intended delay" appears nowhere in the specification. As Synopsys points out, however, the use of the word "initial" suggests that the intended delay may be revised at some point in the process. Indeed, an entire section of the specification addresses the "stretching" and "compressing" of gate delays. (*See* '446 patent at 14:19-15:61.) In particular, "[p]rior to cell placement, the delays of the individual gates may be stretched or compressed to meet the delay constraints[.]" (*See* id. at 14:21-23.) Moreover, claims 12 through 16 of the '446 patent expressly refer to the "stretching" or "compressing" of the "initial intended delay." (*See* id. at 18:14-35.) As Synopsys points out, any definition of "initial intended delay" that requires the delay to be fixed once chosen runs afoul of the plain language of the claims.

Magma's proposal that the "initial intended delay" must remain fixed once selected is based on language describing one embodiment of the invention. (*See* id. at 6:33-57.) In particular, the specification, in describing such embodiment, states that "[d]uring the library analysis 207, the delay D is determined for each gate to be used in the digital circuit," (*see* id. at 6:33-34), and "the gate size is adjusted after cell

placement based on changes in the capacitive load in order to maintain D as 'constant.' " (*See* id. at 6:48-51.) The specification, however, expressly provides that descriptions of particular embodiments are "illustrative only and not in any way limiting" and that "[o]ther embodiments of the invention will readily suggest themselves to those skilled in the art." (*See* id. at 4:55-58.) Given that portions of the specification, as well as the claims themselves, discuss "stretching" or "compressing" the "initial intended delay," the Court agrees with Synopsys that any construction of "initial intended delay" that precludes changes to the delay once selected would be erroneous. FN4 *See* Phillips v. AWH Corp., 2005 WL 1620331 at *15 ("although the specification often describes very specific embodiments of the invention, we have repeatedly warned against confining the claims to those embodiments").

FN4. At his deposition, Magma's expert, Carl Sechen, Ph.D. ("Dr.Sechen"), conceded there is "a possibility" that an initial intended delay could be revised after it is selected. (*See* Boyce Decl. Ex. A (Sechen Dep.) at 35:15-23.)

For the same reason, the Court disagrees with Magma's proposal that the "initial intended delay" must be determined during "library analysis." Although a discussion of "library analysis" appears in the specification in a description of a particular embodiment of the invention, (*see* '446 Patent at 6:26-9:9), the term "library analysis" appears in none of the claims. Moreover, the claims themselves suggest that the determination of the "initial intended delay" may occur at different stages of the process. For example, claim 1 requires that cells be selected from a cell library, and that "at least some of the selected plurality of cells" have "an initial intended delay associated therewith." (*See id*. at 17:14-25.) Claim 21, on the other hand, requires that cells be "selected from a cell library" and that "the electronic circuit description include[ ] an initial intended delay associated with each cell." (*See id*. at 18:45-56.) Synopsys's expert, David Harris, Ph.D. ("Dr.Harris"), attests that it is well known to those of ordinary skill in the art that the "initial intended delay" may be included in or derived from either the electronic circuit description or library analysis. (*See* Harris Decl. para. 32.) According to Dr. Harris, Magma's proposed construction renders claims 21 "self-contradictory," because "an 'initial intended delay' cannot be 'determined during library analysis' and also be included within the 'electronic circuit description.' " (*See id*. para. 49.) Indeed, the specification supports Dr. Harris's view by expressly stating that library analysis "is not dependent on the actual circuit which is being synthesized and thus can be performed separately from the circuit design process[.]" (*See* '446 Patent at 6:30-33.) Dr. Harris further attests that it would make "no sense, in light of the purpose of the invention, to require that the 'initial intended delay' be obtained during library analysis," because "[t]he invention would work just fine for its intended purpose regardless of whether the initial intended delay is specified in the netlist, the delay is calculated during library analysis, or the delay is obtained in some other manner." (*See id*. para. 50.) For all of these reasons, the Court finds there is no limitation that the "initial intended delay" be determined during library analysis.

By contrast, Synopsys's construction of "initial intended delay" as a "delay set as a target" comports with the ordinary meaning of the claim language and the specification. As noted, both the specification and the claims discuss stretching and compressing the "initial intended delay," as necessary, (*see, e.g.,* '446 Patent at 14:19-15:62, 18:14-35), which demonstrates that the "initial intended delay" is an estimate or target, rather than a fixed requirement. The Court also notes that the specification discusses the "initial intended area" of the cells and the "initial intended lengths" of the wires connecting the cells, both of which are subject to change, (*see, e.g.,* '446 Patent at 3:30-37), which further suggests that the "initial intended delay" also may change once selected.

Accordingly, the Court will construe "initial intended delay" as "a delay set as a target."

b. Relative delay value

Disputed Claim Language	Synopsys's Proposed Construction	Magma's Proposed Construction
Relative delay value	a delay value set as a target that may be adjusted relative to another value, such as timing constraints	delay determined during library analysis that is intended to be maintained constant prior to and after placement/routing

The phrase "relative delay value" appears in claims 28, 29, 51 and 52 of the ' 446 patent and claims 1, 12, 13, 14 and 16 of the '438 patent. (*See* ' 446 Patent at 19:24-34, 22:13-31; *see also* '438 Patent at 17:8-27, 18:26-38, 18:42-45.) Magma contends that "relative delay value" has the same meaning as "initial intended delay," while Synopsys contends that the two terms have different meanings.

Other than claim 1 of the '438 patent, each of the claims that contains the term "relative delay value" mentions "stretching" or "compressing" the "relative delay value" of a cell. (*See* '446 Patent at 19:24-34, 22:13-31; *see also* '438 Patent at 18:26-38, 18:42-45.) For example, claim 28 of the ' 446 patent requires the step of "stretching the associated relative delay value of a selected cell after the step of placing and before the step of determining the area." (*See* '446 Patent at 19:26-28.) Claim 1 of the '438 patent, by contrast, does not provide for any change to the "relative delay values." (*See* '438 Patent at 17:8-27.)

As an initial matter, the Court notes that " 'different words or phrases used in separate claims are presumed to indicate that the claims have different meanings and scope.' " *See* Seachange Int'l, Inc. v. C-Cor, Inc., 413 F.3d 1361, 1368 (Fed.Cir.2005) (quoting Karlin Technology Inc. v. Surgical Dynamics, Inc., 177 F.3d 968, 971-72 (Fed.Cir.1999)). Because the claims of the '446 patent include both the phrases "initial intended delay" and "relative delay value," it is presumed that the two phrases have different meanings. "However, the doctrine only creates a presumption that each claim in a patent has a different scope; it is not a hard and fast rule of construction" and cannot be used to "broaden claims beyond their correct scope, determined in light of the specification and the prosecution history and any relevant extrinsic evidence." *See* id. at 1369 (internal quotations and citations omitted).

As Magma correctly points out, the '446 patent application was amended in May 2000 to replace, in some instances, the phrase "relative delay value" with the phrase "initial intended delay." (*See* Huffsmith Decl. Ex. 17 at SY002223.) Magma contends that this substitution indicates the two phrases have the same meaning. FN5 Magma also points out that references to "relative delay value" in the dependent claims of the ' 446 patent are based on independent claims that appear to use the phrase "initial intended delay" to describe the same thing. Specifically, claim 21 of the ' 446 patent refers to "an initial intended delay associated with each cell" and contains no reference to "relative delay value," (*see* '446 Patent at 18:55-56), while dependent claims 28 and 29 describe, respectively, stretching or compressing "the associated relative delay value of a selected cell," and make no mention of "initial intended delay." (*See id*. at 19:24-33.) The Court agrees that "relative delay value" in dependent claims 28 and 29 appears to refer to the "initial intended delay" set forth in independent claim 21. Similarly, independent claim 49 refers to "computing the initial intended delay value of each cell based on the initial intended gain value," while dependent claims 51 and 52 discuss changing the gain value in order to change "the associated relative delay value of said cells." (*See id*. at 22:7-8, 13-20.) The Court agrees with Magma that "relative delay value" in claims 51 and 52

appears to refer to the "initial intended delay" set forth in independent claim 49.

FN5. At his deposition, Dr. Sechen testified that "initial intended delay has units of time, whereas the relative delay value is unitless," but further testified that the difference in measurement of the two terms did not constitute a difference in meaning. (*See* Boyce Decl. Ex. A (Sechen Dep.) at 80:3-15, 85:5-86:1.)

Moreover, the only reference in the specification to "relative delay" appears in the "Summary of the Invention" section, which states that the invention "broadly provides a method for designing an integrated circuit layout based upon an electronic circuit description and by using a cell library containing cells that each have an associated relative delay value[.]" (*See id*. at 3:17-21.) The summary of the invention further provides that "the initial intended area of at least some of the selected plurality of cells" is "determined using the associated relative delay value of the selected cell and the initial intended lengths of some of the wires coupled to the selected cell [.]" (*See id*. at 3:31-35.) Other than in the language of the claims, no other reference to "relative delay value" appears in the '446 or '438 patents. Although Synopsys argues that "relative delay value" is "not an initial delay at all, but rather is a delay that has already been adjusted 'relative to' another value such as the timing constraints in the circuit," (*see* Reply at 10), the claim language, as well as the above-cited language from the specification, contradicts Synopsys's argument. In particular, claim 1 of the '438 patent makes no reference to adjusting the "relative delay value"; rather, it notes that the cells in a cell library already have "an associated relative delay value" when selected from the library, and that the "area" of some of the selected cells is adjusted based on the "relative delay value" of those cells in order meet predetermined timing constraints. (*See* '438 Patent at 17:8-28.) The Court finds there is no distinction in the patent between the "initial intended delay" and the "relative delay value." FN6

FN6. Synopsys concedes that the terms "initial intended delay" and "relative delay value" are "at least similar," as its proposed constructions of the two terms and its own expert's testimony demonstrate. (*See* Harris Decl. para. 93 ("It appears that the parties are in agreement that the 'relative delay value' is at least similar to the 'initial intended delay' set forth in the claims of the '446 Patent.")

Accordingly, the Court will construe "relative delay value" in the same manner as it construed "initial intended delay": "a delay set as a target."

c. Realized

Disputed Claim Language	Synopsys's Proposed Construction	Magma's Proposed Construction
Realized	the delay obtained is less than or approximately equal to the initial intended delay	the initial intended delay of each [some] cell is achieved

Four of the independent claims of the '446 patent, claims 1, 21, 35, and 43, require that the area of some cells be determined so that the "initial intended delay" of said cells is "realized." FN7 (*See* '446 Patent at 17:33, 18:62-63, 20:5-6, 20:58-21:11.) The parties' dispute as to the construction of the term "realized" is based on a disagreement as to whether the initial intended delay must be achieved exactly or whether a faster than anticipated delay is sufficient to "realize" the initial intended delay. Magma contends that the initial intended delay must be "achieved" to be "realized," while Synopsys contends that the initial intended delay is "realized" if "the delay obtained is less than or approximately equal to the initial intended delay."

FN7. Dependent claims 12 through 16 permit the "initial intended delay" to be "stretched" or "compressed" prior to determining the area of the cells. (*See id*. at 18:14-35.)

The purpose of "realizing" the "initial intended delay" is to ensure that "predetermined timing constraints are met." (*See* '446 Patent at 17:23-25, 19:59-61.) The specification of the '446 patent recognizes that timing constraints may be met when the delay is less than intended. It expressly notes that in the prior art, one way of "increasing the probability of meeting timing constraints" is to make the size of the gates larger than necessary, (*see* id. at 1:61-2:3), and further notes that although such an approach "increases the probability of meeting timing constraints," gates that are "larger than the necessary size are wasteful in both silicon area and power consumption," (*see* id. at 1:63-2:1). The invention set forth in the '446 patent is intended to address this problem, (*see* id. at 3:12-13), by permitting the size of each cell to be adjusted during or after placement to more closely achieve the desired delay. (*See* id. at 16:24-26.) Nothing in the specification, however, requires that the cell size be adjusted to exactly achieve the initial intended delay. Indeed, the specification recognizes that timing constraints are met if "slack is zero or positive," FN8 (*see* id. at 13:29-30), and further provides that "it is preferable to maintain a small amount of slack for a path, in order to compensate for downstream delay effects, such as wire delay." (*See* id. at 15:44-46.) FN9

FN8. Dr. Harris attests that "[s]lack is the difference between the actual path delay and the maximum path delay permitted by the timing constraint." (*See* Harris Decl. para. 71.)

FN9. The Court notes that Magma's own expert, Dr. Sechen, testified that "there's a certain goal, ... a certain timing constraint, and then you have to be below it, at or below it." (*See* Boyce Decl. Ex. A (Sechen Dep.) at 32:8-13.)

Accordingly, the Court agrees with Synopsis that the "initial intended delay" is "realized" if "the delay obtained is less than or approximately equal to the initial intended delay."

d. Assigned in buckets

Disputed Claim Language	Synopsys's Proposed Construction	Magma's Proposed Construction
Assigned in buckets	assigned to areas in which items are stored or contained, such as partitions or sectors of a placement area	assigned to fixed-sized two-dimensional regions of the chip area

The phrase "assigned in buckets" appears in claims 17 and 31 of the ' 446 patent and claim 17 of the '438 patent. Claim 17 of the '446 patent states: "The automated method of claim 1 wherein a group of said some cells are assigned in buckets and operated upon ." (*See* '446 Patent at 18:36-37.) Claim 31 states: "The automated method of claim 21 wherein a group of said some cells are assigned in buckets and operated upon in order to determined [sic] the initial intended area of each of the group of said some cells." (*See id*. at 19:38-41.) Claim 17 of the '438 patent states: "The automated method of claim 1 wherein a group of said some cells are assigned in buckets and operated upon in order to determined [sic] the initial intended area of each of the group of said some cells." (*See* '438 Patent at 18:46-49.)

The only discussion of "buckets" in the specification appears in a section of the specification that discusses cell placement in one embodiment of the invention. (*See* '446 Patent at 15:65-16:22.) In such discussion, the specification states:

In step 225 (FIG.4), the placement of cells is performed. FIGS. 10A and 10B show how a circuit design is transformed from a logical hierarchy 830 to a physical hierarchy 832 during the cell placement step 225 (FIG.4). In the physical hierarchy 832, the intermediate logic levels in the logical hierarchy 830 are associated in or grouped in buckets 834 wherein each bucket 834 holds, for example, about one-hundred (100) cells 836. The buckets 834 are arranged in an array as shown in FIG. 10C. If the designer chooses to keep a group of cells 836 together, then the group of cells 836 are grouped in the same buckets 834 or in neighboring buckets. Preferably, a bucket 834 is sized small enough such that cell placement within a bucket 834 has an insignificant effect on timing. In other words, the size of a bucket 834 is such that the wire delay in a bucket 834 can be ignored. However, the size of a bucket 836 should be large enough to accommodate remapping and resizing of the cells 836 contained in the bucket. The number of cells which can be placed within a bucket can range, preferably, from about 20 cells to about 200 cells.

Pre-routes and pre-places (for driving the placer and global router) are driven into the bucket 834 structure. It is further noted, however, that the present invention may be practiced or incorporated with conventional placement methods and systems.

(*See id*.)

Dr. Harris attests, referring to three technical dictionaries, that "bucket" is a term of art in the computer science industry that has been defined as "an area of storage that may contain more than one record," "a storage cell in which data may be accumulated," and "[a]n area of storage where items with a common property are stored." FN10 (*See* Harris Decl. para. 76 and Exs. H, N, and O.) Dr. Harris further attests that the use of the term "buckets" in the specification is "entirely consistent with the normal dictionary definition of the term 'buckets.' " (*See id*. para. 79.)

FN10. Magma's expert, Dr. Sechen, attests that the definitions cited by Dr. Harris "relate to computer storage or memory and are not useful for understanding the meaning of the term 'buckets' in the context of the ' 446 patent." (*See* Sechen Decl. para. 56.) Magma's proposed construction, however, although purportedly tethered solely to the language of the specification, (*see* Magma Mem. at 13), is, as discussed infra, unpersuasive.

In the instant patent, "buckets" are used in the course of placement of cells on an integrated circuit. (*See* '446 Patent at 15:65-16:22.) Said placement is part of the process of transforming the "logical hierarchy" of the chip to a "physical hierarchy." (*See id,* at 15:65-16:1.) According to Dr. Harris, the term "hierarchy" indicates a subdivision of a complex whole into multiple simpler pieces, and the term "physical hierarchy" is "a hierarchy applied to the layout of an integrated circuit." (*See* Harris Decl. para. 79 and n. 1.) Dr. Harris further attests that, "[a]s is known to one of ordinary skill in the art, the physical hierarchy is a subdivision of the whole placement area into partitions or sectors." (*See id*.) Synopsys's proposed construction of "buckets" as "areas in which items are stored or contained, such as partitions or sectors of a placement area" thus applies the standard technical dictionary definition of "bucket" and applies it to the specific field of integrated circuit design.FN11

FN11. Dr. Harris also points out that another Magma patent, in which van Ginneken likewise is a listed inventor, discusses grouping cells in buckets and defines "buckets" as "sectors in the placement area." (*See id*. para. 81 and Ex. P (United States Patent No. 6,230,304 ('304 patent)) at 7:32-35.) There is no argument that the prosecution history of the ' 304 patent has any relationship to the prosecution of the '446 patent and, consequently, the Court is hesitant to define a term in the '446 patent by reference to the usage of such term in another, unrelated, patent. Nonetheless, the Court agrees with Dr. Harris that the usage of the term "bucket" in the '304 patent comports with the technical dictionary meaning of the term, and nothing in the specification of the '446 patent suggests that a non-standard meaning of "bucket" was contemplated by the inventor.

Magma's proposed claim construction, requiring "buckets" to be "fixed-sized two-dimensional regions of the chip area," is not supported by the claim language, the specification, or the dictionary definitions cited by Dr. Harris. Magma relies on the statement in the specification that the buckets "are arranged in an array as shown in FIG. 10C," and points to the uniform grid set forth in that figure as evidence that the buckets must be both fixed in size and arranged in a two-dimensional array. (*See* '446 patent at 16:5-6 and Fig. 10C.) Although Figure 10C is the only figure in the '446 patent depicting the arrangement of buckets on a chip, nothing in the specification requires that the buckets be either fixed in size, or arranged in a two-dimensional array. As noted, the Federal Circuit has "expressly rejected the contention that if a patent describes only a single embodiment, the claims of the patent must be construed as being limited to that embodiment." *See* Phillips v. AWH Corp., 2005 WL 1620331 at *15.

Accordingly, the Court will adopt Synopsys's proposed construction and will construe "assigned in buckets" as "assigned to areas in which items are stored or contained, such as partitions or sectors of a placement area."

B. The '114 Patent

The '114 patent is titled "Method For the Physical Placement of an Integrated Circuit Adaptive to Netlist Changes." The invention set forth in the '114 patent "relates to a method for the physical placement of an integrated circuit chip that is adaptive to changes made to a netlist." (*See* ' 114 Patent at 1:7-9.)

As set forth in the "Background" section of the '114 patent, the design of any integrated circuit typically "begins with an engineer conceiving and defining the performance specification of the new IC chip." (*See* id. at 1:27-29.) "A high level language is used to translate this specification into functional criteria which are fed into a logic synthesis program," which "generates a netlist containing a collection of gates," also known as "cells." (*See* id. at 1:29-32.) The netlist "can be regarded as a template for the realization of the physical embodiment of the integrated circuit in terms of transistors, routing resources, etc." (*See* id. at 1:34-36.) "Next, a physical design tool is used to place and route the IC chip" by determining "the physical pinouts, wiring, interconnections and specific layout of the semiconductor chip." (*See* id. at 1:1:37-40.)

"As the complexity, functionalities, speed, and size of these chips increase, it is becoming a much more critical and difficult task to properly design, layout, and test the next generation of chips." (*See* id. at 1:50-54.) The '114 patent notes the following problems with the processes described in the prior art:

Often, several iterations of the design, layout, and testing process are required in order to optimize the

semiconductor chip's size, cost, heat output, speed, power consumption, and electrical functionalities. However, one problem is attributable to the fact that each of these stages is highly dependent on the results of the other stages. A minor alteration in one stage intended to enhance one characteristic may cause unforeseen problems to occur in other stages. For example, changing a cell in the synthesis stage might drastically alter the current place and route. It is this high degree of interdependence which makes it extremely difficult to predict and account for the consequences associated with any changes. Indeed, the overall design might sometimes be worse in a successive iteration. Furthermore, the iterative process is time-consuming and requires a powerful computer to perform the processing. In addition, the iterative process is labor intensive and requires the dedication of a highly skilled, experienced EDA specialist.

(*See* id. at 1:54-2-4.) The invention set forth in the '114 patent is intended to "cut[ ] the cost and time associated with the semiconductor chip design process, while at the same time, allow[ing] a designer to optimize the chip's performance." (*See* id. at 2:5-9.)

The '114 patent summarizes the invention as follows:

The present invention pertains to a computer controlled method for the rough placement of cells in the design of integrated circuits. Initially, a synthesis tool is used to generate a netlist according to HDL,FN12 user constraint, and technology data. Thereupon, a cell separation process assigns (x,y) locations to each of the cells. The cell location information is supplied to the synthesis tool, which can then make changes to the netlist thereto. In the present invention, the size of the placement area is allowed to be scaled according to the new netlist. Next, the cells of the netlist are spaced apart according to a spacing algorithm. A partitioning algorithm is then applied to group the cells into a plurality of partitions. A number of iterations of cell separation, synthesis of new netlist, size adjustment (if necessary), spacing, and partitioning are performed until the cells converge. Thereupon, detailed placement and routing processes are used to complete the layout.

FN12. "HDL" stands for "hardware design language." (*See* id. at 4:64.)

(*See* id. at 2:12-28.) During the prosecution of the '114 patent, the inventors stated: "The significance of this invention is that by allowing netlist changes to be entered during the rough placement process, the overall number of iterations required for the design of integrated circuits is minimized." (*See* Harris Decl. Ex. Y at 6.)

1. Convergence criterion based upon a partition size

Disputed Claim Language	Synopsys's Proposed Construction	Magma's Proposed Construction
Convergence criterion based upon a partition size	a condition based upon a partition size that would, if satisfied, achieve a predetermined result	condition for terminating an iterative process based on the number of cells contained in a partition
Partition size	Number of cells in a partition or the total area of cells in a partition	Number of cells contained in a partition

The phrase "establishing a convergence criterion based upon a partition size" appears in claims 1, 6, and 11 of the '114 patent. For example, claim 1 states:

In the design of integrated circuits, a computer controlled method for placing cells in a placement area, comprising:

generating a netlist through a synthesis process;

establishing a convergence criterion based upon a partition size;

executing a cell separation process according to the netlist;

changing the netlist in response to how the cells are placed;

modifying the spacings of the cells responsive to changes made to the netlist;

partitioning the cells into a plurality of partitions; and,

determining whether the partitions meet said criterion for convergence.

(*See* '114 Patent at 6:56-7:3.) The key disputes between the parties with respect to the construction of this term relate to (1) whether "partition size" is limited to the number of cells contained in a partition or whether it also encompasses the total area of cells in a partition, and (2) whether "convergence criterion" applies only to an iterative process or whether it can apply to a process that can be completed in only one attempt.

In the preferred embodiment of the invention, a five-step process occurs during the "rough placement process." (*See id*. at 3:8-15, 3:47.) The five steps are (1) cell separation, (2) changing the netlist, (3) changing the spacings, (4) partitioning the cells, and (5) determining whether the then-current placement "has successfully converged." (*See id*. at 3:14-61.) In the fourth step, according to the specification, "[p]artitioning refers to the process of subdividing the cells in order to better 'spread' them apart." (*See id*. at 3:48-49.) In step four, "the partitions are defined"; then, in step five, "a determination is made as to whether the current placement has successfully converged." (*See id*. at 3:47, 3:52-54.) In the preferred embodiment,

Convergence is achieved when each of the partitions reaches a pre-determined size. For example, the user can set the convergence point to occur whenever each of the partitions is comprised of less than twenty gates.

(*See id*. at 3:54-57.) If convergence has not been reached, the first four steps are repeated. (*See id*. at 3:57-58.) "Otherwise, once convergence has been achieved, the detailed placement and route process is performed to complete the physical layout." (*See id*. at 3:59-61.)

Although the description of the preferred embodiment cited above describes the size of the partitions by reference to the number of gates or cells contained therein, nothing in the specification requires partitions to be measured in that manner. *See* Phillips v.. AWH Corp., 2005 WL 1620331 at *15 ("[A]lthough the specification often describes very specific embodiments of the invention, we have repeatedly warned against confining the claims to those embodiments.") Indeed, the claims demonstrate that measuring the size of the partitions by reference to the number of cells contained therein is only one method of measuring the size of the partitions. In particular, independent claim 1 states that the convergence criterion is "based upon a

partition size," without stating any particular method of determining partition size; the only difference between independent claim 1 and dependent claim 5 is that in claim 5, "the partition size is measured by the number of gates contained therein." (*Compare* '114 Patent at 6:56-7:3 (claim 1) *with id*. at 7:11-12 (claim 5).) Under the doctrine of claim differentiation, "different words or phrases used in separate claims are presumed to indicate that the claims have different meanings and scope," and the doctrine "is at its strongest where the limitation sought to be read into an independent claim already appears in a dependent claim." *See* Seachange Int'l, Inc. v. C-Cor, Inc., 413 F.3d at 1368-69 (internal quotations and citations omitted). Were the Court to adopt Magma's proposed construction, claim 1 and claim 5 would be identical.

Moreover, the specification states that the number of cells in each partition is "approximately the same" and the area of each partition "is proportional to the area of the cells included in it." (*See* '114 Patent at 4:45-47.) As the '114 patent expressly notes that the sizes of cells may be changed, (*see* id. at 3:21-22), there can be no assumption that all cells are the same size. Consequently, there is no way to ensure that the area of the partition is "proportional to the area of the cells included in it" without, in fact, measuring the size of the partition by reference to the area of the cells. Consequently, Synopsys's proposed construction of "partition size" as being measured by either the "number of cells in a partition or the total area of cells in a partition" is supported by the specification and the Court will adopt that construction.

With respect to "convergence criterion," the specification states that, in the preferred embodiment, "convergence" is reached once the partitions reach a specified size. (*See* id. at 3:54-55 .) Thus, in that example, the "convergence criterion" is the specified size of the partitions. In the preferred embodiment, the purpose of the "convergence criterion" is to determine when to perform "the detailed placement and route process ... to complete the physical layout," (*see* id. at 3:59-61); the specification notes, however, that the invention "can be applied to any one of several phases associated with the physical route and placement of an IC design," (*see* id. at 3:8-10). Thus, it is clear that "convergence criterion" is not limited to the specific example discussed in the specification, and no party argues for such a limitation.

The example in the specification suggests, nonetheless, that the convergence criterion is intended to be a condition which, when achieved, triggers the next step in the process. In the example set forth in the specification, once the steps of (1) "cell separation," (2) "tweak[ing]" the netlist, (3) "changing the spacings," and (4) "partitioning" the cells, are completed, "a determination is made as to whether the current placement has successfully converged," i.e., whether the partitions have reached the desired size. (*See* id. at 3:14-55.) If so, "the detailed placement and route process is performed to complete the physical layout"; if not, the first four steps are repeated until the partitions reach the desired size, i.e., the "convergence criterion ." (*See* id. at 3:57-61.)

Magma argues that the term "convergence criterion" can only apply to an iterative process, i.e., a process that repeats until a desired result is reached. Magma's expert, Majid Sarrafzadeh, Ph.D. ("Dr.Sarrafzadeh"), attests that "the phrase 'convergence criteria' ... necessarily refers to an iterative process" and not to a "direct process that is designed to solve the problem in one pass (i.e., in a known number of steps)." (*See* Sarrafzadeh Decl. para.para. 21-22.) Dr. Sarrafzadeh characterizes "optimization methods," such as the process of "arranging transistors in a computer chip so that the resulting layout occupies the smallest area and uses the smallest number of components," as either "direct" or "iterative." (*See* id. at para.para. 17-18.) According to Dr. Sarrafzadeh, "direct" methods are those that "produce an answer in a fixed number of computational steps," while "iterative" methods are those that "produce a sequence of approximate answers, designed to converge ever closer to an optimal solution under the proper conditions." (*See* id. at para. 18.) An "iterative process," Dr. Sarrafzadeh attests, consists of "a sequence of steps that is repeated, or iterated,

until some specified result is achieved." (*See* id. at para. 20.) Dr. Sarrafzadeh further attests that the "rate at which an iterative process gets closer to the desired end result is called the 'convergence rate'." (*See* id. para. 20.) Where iterative processes are used to address complex problems, Dr. Sarrafzadeh attests, there is no guarantee that the optimal point will be found in an acceptable amount of time; consequently, a "termination constraint" or "convergence criterion" must be set so that the process "will terminate when it generates an intermediate result that is close enough to the optimal point." (*See* id.)

According to Dr. Sarrafzadeh, a "direct process," by contrast, "does not make small improvements to the answer gradually with the goal of converging on the desired result." (*See* id. para. 22.) Rather, Dr. Sarrafzadeh attests, a "direct process is designed to run through a known set of steps once and produce the result generated at the end of the entire process" and "[o]nly at the end of execution of the algorithm can the output be realized." (*See* id. para. 22.) Thus, in Dr. Sarrafzadeh's opinion, "there can be no concept of establishing criteria to identify when an intermediate result has come close enough to the desired result so that the process should be terminated" and "there is no concept of convergence criteria for a direct or non-iterative process." (*See* id. para. 23.) Further, according to Dr. Sarrafzadeh, "a person of ordinary skill in the art would have used the term 'convergence' only to refer to an iterative method, and the term 'convergence criteria' to refer to conditions for terminating an iterative process." (*See* id. para. 29.) Dr. Sarrafzadeh notes that the "Summary of the Invention" section of the '114 patent expressly states that "[a] number of iterations of cell separation, synthesis of new netlist, size adjustment (if necessary), spacing, and partitioning are performed until the cells converge." (*See* '114 Patent at 2:25-28.) The specification, Dr. Sarrafzadeh notes, also describes the act of partitioning as an iterative process:

The cells are partitioned first into two groups, then into four, then into eight, and so on, until there are only a few cells in each group.... If each of these partitions ... is small enough to meet a particular criteria set by the user, convergence is declared.

(*See id*. at 4:41-43, 4:52-53.) Dr. Sarrafzadeh thus concludes that the "convergence criteria" must be defined as referring to "conditions for terminating an iterative process." (*See* Sarrafzadeh Decl. para. 29.)

Synopsys's expert, Dr. Harris, recognizes that the inventors of the '114 patent explained to the PTO that the significance of their invention was that "the overall number of iterations required for the design of integrated circuits is minimized." (*See* Harris Decl. para. 125 and Ex. Y at 6.) Dr. Harris argues, however, that there is no requirement in the '114 patent that the iterative process described in the '114 patent be performed more than once because, ideally, if the convergence criterion is met after the first iteration, there is no need to repeat the process. (*See* id. para.para. 126-128.) Although the Court agrees that there is no requirement that the process actually repeat before the convergence criterion is met, the process itself is still iterative in that it is designed to repeat until the convergence criterion is met. (*See, e.g.,* '114 Patent at 3:57-58 ("If convergence has not been reached, steps 103-106 are repeated.")).

For the reasons set forth above, the Court will adopt Synopsys's proposed construction of "partition size" and Magma's proposed construction of "convergence criterion." Accordingly, the Court will construe "convergence criterion based upon a partition size" as "condition for terminating an iterative process based on the number of cells contained in a partition or the total area of cells in a partition." For clarity, the Court will define "iterative process" as "a sequence of steps that is intended to be repeated until some specified result is achieved." (*See* Harris Decl. para. 104; Sarrafzadeh Decl. para. 20.)

2. Cell separation process

Disputed Claim Language	Synopsys's Proposed Construction	Magma's Proposed Construction
Cell separation process	a process which assigns a cell a location or an approximate location on the physical placement area	method of assigning locations to cells such that they do not overlap

The phrase "cell separation process" appears in claims 1, 6, and 11 of the '114 patent, each time as part of the longer phrase "executing a cell separation process according to the netlist." (*See* '114 Patent at 6:56-7:3, 7:13-28, 8:5-22.) The parties agree that the "cell separation process" involves assigning a location to the cells, but dispute whether the cells are assigned to specific, as opposed to approximate, locations, and whether cells may overlap in any way.

In the initial portions of the '114 patent specification, one possible reading of the language is that the "cell separation process" assigns specific locations to cells but does not require that the cells be spaced apart from each other. For example, the "Summary of the Invention" section of the '114 patent states:

[A] cell separation process assigns (x,y) locations to each of the cells. The cell location information is supplied to the synthesis tool, which can then make changes to the netlist thereto. In the present invention, the size of the placement area is allowed to be scaled according to the new netlist. Next, the cells of the netlist are spaced apart according to a spacing algorithm.

(*See* '114 Patent at 2:16-23.) Additionally, in the "Detailed Description" portion of the specification, which describes a preferred embodiment of the invention, the inventors reiterate that "cell separation" and "spacing" are separate steps of the patented process. (*See id*. at 3:14-20, 3:41-47.) According to the specification, "[t]he cell separation process takes each cell in the netlist and assigns a pair of (x,y) coordinates" which are "used to specify the location of each cell relative to a two-dimensional boundary area in which the circuit is to be placed." (*See id*. at 3:16-20.) The placement of cells during the "cell separation process" is "a best estimate guess," after which "the netlist is tweaked to optimize the design." (*See id*. at 3:27-32.) Only thereafter does the "spacing" of the cells occur, followed by a separate step of partitioning the cells "in order to better 'spread' them apart." (*See id*. at 3:41-48.) The above-cited language arguably suggests that the "cell separation process" includes the step of assigning a location to each cell, but does not include the step of ensuring that the cells are "spaced apart." FN13

FN13. Alternatively, this language can be read as requiring separation, i.e., non-overlap, followed by improved spacing "according to an algorithm," or formula.

Elsewhere in the specification, however, in a more detailed description of "cell separation" found in a description of a preferred embodiment, the specification expressly states that "[c]ells *must* be assigned locations so that they do not overlap each other, they all fit within some overall bounding figure, and the total wiring cost is minimized." (*See id*. at 5:23-25 (emphasis added).) The cell separation process determines "an assigned (x,y) position ... denoting the approximate centerpoint of the cell." (*See id*. at 5:27-28.) The specification further explains that, in the spacing step, the partition walls are changed "in order to improve the spacings between the cells." (*See id*. at 5:32-35 (emphasis added).) Although the above-cited language appears in the description of a preferred embodiment, (*see id*. at 4:59-61), the provision that, during cell separation, "[c]ells must be assigned locations so that they do not overlap each other," read in context, describes a requirement of the invention rather than an optional aspect of the preferred

embodiment.

Nonetheless, Dr. Harris attests, "[t]o one with ordinary skill in the art, it would make no sense to require that the cells are completely non-overlapping" at the conclusion of the cell separation process. (*See* Harris Decl. para. 134.) He further attests that while "it is true that the precise x,y locations for the centerpoints of two cells need to be different (because one cannot have two cells that have precisely the same centerpoint), this does not mean that the entire area of the cells must or should be non-overlapping." (*See id*.) According to Dr. Harris, "it is typical during rough placement, that cells are assigned overlapping locations, and this overlap is usually dealt with during detailed placement." (*See id*. para. 138.)

Even if it is "typical" for cells to overlap during rough placement, the specification of the '114 patent expressly states, as noted, that "[c]ells must be assigned locations so that they do not overlap each other." (*See* ' 114 Patent at 5:23-25.) The Federal Circuit has held that "the specification may reveal an intentional disclaimer, or disavowal, of claim scope by the inventor" and, in such instances, "the inventor has dictated the correct claim scope, and the inventor's intention, as expressed in the specification, is regarded as dispositive." *See* Phillips v. AWH Corp., 2005 WL 1620331 at *8. Accordingly, the Court concludes that the "cell separation process" must result in assignment of cells to locations such that they do not overlap each other in any way.

With respect to whether the cells are assigned to precise locations during the "cell separation process," the specification repeatedly states that the cells are assigned "(x,y)" locations during the cell separation process. (*See, e.g.,* '114 Patent, Abstract and 2:17-18, 3:16-17, 5:12-14, 5:25-28.) Synopsys's argument that the locations nonetheless may be approximate is based entirely on one sentence in the specification: "The output from cell separation process 306 is a number of cells, each of which has an assigned (x,y) position 307 denoting the approximate centerpoint of the cell." (*See id*. 5:25-28.) As Dr. Sarrafzadeh suggests, however, where a cell has an irregular shape, its precise centerpoint may be difficult to determine, and the cell nonetheless is assigned to a precise (x,y) location, which location is intended to represent the "approximate centerpoint" of the cell. (*See* Sarrafzadeh Decl. para. 43; *see also* '114 Patent at 5:25-28.) Synopsys fails to explain how a cell can be assigned to specific (x,y) coordinates and still be assigned only an "approximate" location.

Accordingly, the Court will adopt Magma's construction of "cell separation process" and construe the term as "a method of assigning locations to cells such that they do not overlap."

3. Partitioning the cells into a plurality of partitions

Disputed Claim Language	Synopsys's Proposed Construction	Magma's Proposed Construction
Partitioning the cells into a plurality of partitions	subdividing or distributing the cells into more than one partition	subdividing cells in one region into multiple groups of cells

The phrase "partitioning the cells into a plurality of partitions" appears in claims 1, 6, and 11 of the '114 patent. The parties' dispute as to the construction of this term relates to whether "partitioning" is limited to subdividing a group of cells from a single region, or whether it also encompasses distributing cells to different partitions without moving the partition boundaries. In other words, if one analogizes a group of cells to a cherry pie, the dispute is whether the pie is "partitioned" only by cutting it into slices, or whether it also may be "partitioned" by moving individual cherries from one location in the pie to a different location in the pie.

The "Summary of the Invention" section of the '114 patent sets forth no requirement that the cells be partitioned in any particular manner, providing only that "[a] partitioning algorithm is then applied to group the cells into a plurality of partitions." (*See* '114 Patent at 2:23-25.) The specification of the '114 patent, however, expressly defines "partitioning" as "the process of subdividing the cells in order to better 'spread' them apart." (*See* id. at 3:48-49.) The specification nevertheless does go on to note that "[t]here are a number of different petitioning approaches that can be implemented with the present invention," citing two articles by name. (*See* id. at 5:38-56.) The patent also provides that "[o]ther approaches to the partitioning process include min-cut, force-directed, simulated annealing, and spectral approaches." (*See* id. at 5:56-58.)

Magma argues that "partitioning," in the context of the '114 patent, requires "subdividing" the cells, i.e., dividing a group of cells into smaller parts, rather than distributing cells to different locations. As Magma notes, in a description of the preferred embodiment, "partitioning" is conducted as follows: "A cell (e.g., in the shape of a rectangle) is broken into two roughly equal sizes by drawing either a horizontal or vertical line through the approximate midpoint." FN14 (*See* id. at 3:49-52.) In the preferred embodiment,

FN14. It appears, based on the context of this statement, that partitioning applies to a group of cells, rather than to a single cell.

[t]he first step of partitioning divides the n cells into two sets of n/2 cells. The number of cells in each side is approximately the same. The area of each half is proportional to the area of the cells included in it. The next step of partitioning is to divide each of these groups in two, this time on the other axis. This process continues until there are only a few cells in each group (e.g., twenty or less).
(*See* id. at 4:43-50.) The above-cited language essentially describes partitioning contiguous groups of cells in the same manner as one might cut a pie into slices.
Synopsys argues that Magma's construction ignores an embodiment described in the '114 Patent in which, according to Dr. Harris, "it is not necessary to draw additional horizontal and vertical lines for subdividing the cells." (*See* Harris Decl. para. 143 (citing '114 Patent at 4:28-36).) The '114 patent recognizes that during the various iterations of the rough placement process, additional cells might be added to the netlist, (*see* id. at 3:20-26), and that despite "efficient partitioning," "there might come a point where there is not enough room to add an additional cell." (*See* id. at 4:21-24.) According to the specification: "The present invention overcomes this limitation whereby, the total area is allowed to expand in order to accommodate additional nets and/or cells." (*See* id. at 4:24-26.) The embodiment cited by Dr. Harris is described in Figure 2 of the '114 Patent:

An example of an expanded area is shown as 213. Expanding the total area affects the partitioning. For example, the location of vertical cutline 214 corresponding to the original area size is now moved to location 215 in order to account for the increase in size as the width of the original boundary 216 is increased by shifting the right boundary to location 217. A change in the partitioning might lead to different placements. For example, prior to enlarging the area, cell 218 belonged to the rightmost partition. After the enlargement, cell 218 now belongs to the leftmost partition.

(*See* id. at 4:26-36 and Fig. 2.) Dr. Harris attests that "[t]his is a technique of subdividing the cells, where, as a result of shifting the partition boundary, the cells in two different regions are redistributed among each other to form two new partitions," and said technique "does not involve the drawing [of] either horizontal or vertical lines in one region." (*See* Harris Decl. para. 143.)

The process described by Dr. Harris, however, is not part of the partitioning process itself, but rather, as Magma argues, a process that occurs during the step of "spacing" the cells in response to changes in the netlist.FN15 (*See* '114 Patent at 3:20-47, 5:33-35; *see also* Dr. Sarrafzadeh. Decl. para. 54.) Further, in such process, although cells may be reassigned from one partition to another, such reassignment again is accomplished by moving partition boundaries, not by moving the cells themselves.FN16 In sum, the process cited by Dr. Harris not only does not result in "distributing" cells from one area to another, it is not part of partitioning at all.

FN15. The Court notes that each of the claims that contains the step of "partitioning the cells into a plurality of partitions" also includes the step of "modifying the spacings of the cells responsive to changes made to the netlist." (*See* '114 Patent at 6:66-67, 7:24-25, 8:18-19.)

FN16. By expanding the area in order to modify the space between cells, the preexisting partition boundaries necessarily move to ensure that the partitions remain of equal size. (*See id*. at 4:22-36, 4:45-47.)

Moreover, although the specification expressly notes that "[t]here are a number of different partitioning approaches that can be implemented with the present invention," and although the patent expressly identifies a number of different approaches, (*see id*. at 5:38-40), Synopsys presents no evidence that any of these methods involves distributing rather than subdividing groups of cells. Magma, by contrast, presents evidence that one of the articles cited in the '114 patent, "A Procedure for Placement of Standard-Cell VLSI Circuits," (*see* '114 Patent at 5:49-50), discusses partitioning cells by "divid[ing]" cells, rather than distributing them.FN17 (*See* Sarrafzadeh Decl. para. 50 and Ex. 33.) Dr. Sarrafzadeh also cites his own textbook, "An Introduction to VLSI Physical Design," in which he states that "[p]artitioning is the task of dividing a circuit into smaller part," and includes a diagram that depicts a group of cells being subdivided. (*See id* . para. 51 and Ex. 34.) Dr. Sarrafzadeh further attests that it would be "completely unusual" to use the term "partitioning" to describe "merely moving cells around between two partition[s]," and that "the specification of the ' 114 Patent is consistent with the ordinary use of the term partitioning to mean subdividing." (*See* id. para. 53.)

FN17. Dr. Sarrafzadeh does not discuss the other methods of partitioning set forth in the '114 patent.

In his reply declaration, Dr. Harris points to two articles which, he contends, show that "one may 'partition' by redistributing cells between existing regions." (*See* Harris Reply Decl. para. 61 and Exs.C and D.) Neither article is cited in the '114 Patent, however, and Dr. Harris has not opined that any of the methods of partitioning that are cited in the '114 Patent involve redistributing cells, rather than subdividing groups of cells.

Accordingly, as the patent specifically defines "partitioning" as "the process of subdividing the cells in order to better 'spread' them apart," (*see* '114 Patent at 3:48-49), and as there is no evidence that any of the particular methods of partitioning cited in the patent involve distributing cells, rather than subdividing groups of cells, the Court will adopt Magma's construction and construe the phrase "partitioning the cells into a plurality of partitions" as "subdividing cells in one region into multiple groups of cells."

CONCLUSION

For the reasons set forth above, and for good cause shown, the Court construes the disputed terms of the patents as follows:

'446 and '438 Patents	
Disputed Claim Language	Court's Construction
Initial intended delay	a delay set as a target
Realized	the delay obtained is less than or approximately equal to the initial intended delay
Assigned in buckets	assigned to areas in which items are stored or contained, such as partitions or sectors of a placement area
Relative delay value	a delay set as a target

'114 Patent	
Convergence criterion based upon a partition size	condition for terminating an iterative process based on the number of cells contained in a partition or the total area of cells in a partition; an "iterative process" is a sequence of steps that is intended to be repeated until some specified result is achieved.
Partition size	the number of cells in a partition or the total area of cells in a partition
Cell separation process	a method of assigning locations to cells such that they do not overlap
Partitioning the cells into a plurality of partitions	subdividing cells in one region into multiple groups of cells

IT IS SO ORDERED.

N.D.Cal.,2005.
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