United States District Court,
E.D. Texas, Beaumont Division.

MOTOROLA, INC,
v.
ANALOG DEVICES, INC.

No. 1:03-CV-131

June 17, 2004.

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MEMORANDUM OPINION AND ORDER CONSTRUING CERTAIN CLAIMS OF UNITED STATES PATENT NO. 5,084,814 (VAGLICA)

RON CLARK**, District Judge.**

Plaintiff, Motorola, Inc. ("Motorola"), filed suit claiming infringement of five patents by Analog Devices, Inc. ("A.D.I."). A.D.I. counter-claim alleging infringement by Motorola of six other patents. All of the patents involve various aspects o microchip production, manufacture, programming, or design. On January 21, 2003, the court conducted a hearing for the purpose of hearing evidence and argument that would assist the court in interpreting the meaning of disputed claims. In two previous orders the court construed the disputed claims in ten of the patents. Turning now to the Vaglica patent. U.S. Patent No 5,084,814, and having carefully considered the parties' briefs, the testimony, and exhibits admitted into evidence, the referenced patents, and the arguments of counsel, the court now makes the following findings and construes the disputed terms as follows:

STANDARD FOR CONSTRUING CLAIM TERMS

In Markman v. Westview Instruments, Inc., 52 F.3d 967 (Fed.Cir.1995) ("*Markman I*"), the Federal Circuit

held that claim construction is a matter of law. In affirming this decision, the Supreme Court in Markman v. Westview Instruments, Inc., 517 U.S. 370, 116 S.Ct. 1384, 134 L.Ed.2d 577 (1996) ("*Markman II*"), stated, "[W]e hold that the construction of a patent, including terms of art within its claims, is exclusively within the province of the court," Id. at 1387, and "... judges, not juries, are the better suited to find the acquired meaning of patent terms." Id. at 1395.

The duty of the trial judge is to determine the meaning of the claims at issue, and to instruct the jury accordingly. In the exercise of that duty, the trial judge has an independent obligation to determine the meaning of the claims, notwithstanding the views asserted by the adversary parties, (citations omitted)

Exxon Chemical Patents, Inc. v. Lubrizoil Corp., 64 F.3d 1553, 1555 (Fed.Cir.1995).

In performing this duty, this court is guided by several principles. The claims should be construed in light of the ordinary meaning of the claim language, as well as the patent specification and prosecution history. Markman I, 52 F.3d at 979-80; *see also* Vitronics Corp. v. Conceptronic, Inc. 90 F.3d 1576, 1582 (Fed.Cir.1996).

The court should first determine the ordinary meaning of a disputed term. There is a "heavy presumption" that the terms used in claims "mean what they say and have the ordinary meaning that would be attributed to those words by persons skilled in the relevant art." Tex. Digital Sys., Inc. v. Telegenix, Inc., 308 F.3d 1193 (Fed.Cir.2002).

It is well established that courts are to determine the plain, ordinary meaning of a claim term *before* turning to the specification. As the Federal Circuit has stated:

... consulting the written description and prosecution history as a threshold step in the claim construction process, *before* any effort is made to discern the ordinary and customer meanings attributed to the words themselves, invites a violation of our precedent counseling against importing limitations into the claims." Tex. Digital, 308 F.3d at 1204 (emphasis supplied).

It is entirely appropriate for a court to look to dictionaries to determine the plain and ordinary meaning of a disputed claim term. *Id*. at 1202.

A dictionary is not prohibited extrinsic evidence, and is an available resource of claim construction. Although a dictionary definition may not enlarge the scope of a term when the specification and the prosecution history show that the inventor, or recognized usage in the field of the invention, have given the term a limited or specialized meaning, a dictionary is often useful to aid the court in determining the correct meaning to be ascribed to a term as it was used.

Vanguard Products Corp. v. Parker Hannifin Corp., 234 F.3d 1370, 1372 (Fed.Cir.2000).

Then, the court should look to the intrinsic evidence of record, that is, the patent specification, and, if in evidence, the prosecution history, to determine whether the patentee clearly intended a meaning different from the ordinary meaning or whether he clearly disavowed the ordinary meaning in favor of some special meaning. *See* Markman I, 52 F.3d at 979.

Claim terms take on their ordinary and accustomed meanings unless the patentee demonstrated a "clear

intent" to deviate from the ordinary and accustomed meaning of a claim term by redefining the term in the patent specification. Johnson Worldwide Assoc., Inc. v. Zebco Corp., 175 F.3d 985 (Fed.Cir.1999).

Claims must be read in view of the specification, of which they are a part. Autogiro 384 F.2d at 397, 155 USPQ at 702; *see* Winans v. Denmead, 56 U.S. (15 How.) at 338; *Bates v. Coe,* 98 U.S. at 38-39. The specification contains a written description of the invention that must enable one of ordinary skill in the art to make and use the invention. For claim construction purposes, the description may act as a sort of dictionary, which explains the invention and may define terms used in the claims.

Markman I, 52 F.3d at 979.

The Federal Circuit offered guidance on how the written description can be helpful in determining the meaning of claims in Scimed Life Systems v. Advanced Cardiovascular, 242 F.3d 1337 (Fed.Cir.2001).

While it is true, of course, that "the claims define the scope of the right to exclude" and that "the claim construction inquiry, therefore, begins and ends in all cases with the actual words of the claim," Renishaw PLC, 158 F.3d at 1248, 48 USPQ 2d at 1121, the written description can provide guidance as to the meaning of the claims, thereby dictating the manner in which the claims are to be construed, even if the guidance is not provided in explicit definitional format.

The patentee may also deviate from the plain and ordinary meaning by characterizing the invention in the prosecution history using words or expressions of manifest exclusion or restriction, representing a "clear disavowal" of claim scope. Teleflex, Inc. v. Ficosa N. Am. Corp., 299 F.3d 1313, 1327 (Fed.Cir.2002). However, absent a "clear indication" from the patent specification or a "clear disavowal" in the prosecution history, there is a "heavy presumption" that a claim term is given its plain and ordinary meaning. Tex. Digital, 308 F.3d at 1202.

Extrinsic evidence maybe considered if needed to assist in determining the meaning or scope of technical terms in the specification or claims to one of ordinary skill in the art. *Vitronics* at 1583.

THE VAGLICA PATENT

U.S. Patent No. 5,084,814, the Vaglica Patent, was issued on January 28, 1992, and is held by Mototola. The Vaglica patent relates to the "debugging" of computer programs. A computer program is basically a series of instructions to a computer, with each instruction causing the computer to perform a specific task. The computer typically executes these instructions one at a time. Many programs have errors, or "bugs," that cause them to perform incorrectly, and programmers commonly test programs to find and correct, or "debug," the programs, In the Vaglica patent, the data processor can operate in two modes. In one mode, the processor executes instructions in a normal manner, for example, when executing a user program. In the second mode, the normal execution of instructions is halted, and debug instructions are received and executed by the processor. The Vaglica processor includes a special communication port that can be used to convey debug instructions to the processor.

Disputed Claim Terms of the Vaglica Patent

Claims 8, 10, 13, 14, 17 and 20 from the Vaglica patent are asserted in this case. These are copied as Exhibit A on the next page.

"data processor/data processing system"-claims 8, 10, 13, 14, 17, & 20

The term "data processor" is found in claims 8, 13, 14, 17, and 20 and the phrase "data processing system" is found in the preamble of claim 10. As claim 10 depends from claim 8, it is clear that the phrase "data processing system" refers to the "data processor" referenced in the preamble of claim 8, and the two terms will be construed identically.

Motorola proposes that the phrases be construed to mean "a device that can execute a set of instructions and that can be programmed to execute the instructions." ADI proposes that the phrases be interpreted as "an integrated circuit including a microprocessor." Motorola argues initially that, because these terms are only found in the preamble of the various claims and not in the body of the

EXHIBIT A

Patent Number: 4,084,814
Vaglica et al.

1. A data processor for executing each of a plurality of instructions, the data processor having a plurality of system resources and comprising:

first means for executing said instructions;

second means for utilizing the system resources in accordance with the execution by said first means of a first subset of said instructions;

third means for providing access to at least one of the system resources in accordance with the execution by said first means of a second subset of said instructions;

first communication means for providing instructions of said first subset to said first means, said first communication means is operative for communication in response to instructions of both said first and second subsets of instructions;

second communication means distinct from said first communication means for providing instructions of said second subset to said first means, said second communication means is not operative for communication of instructions of said second subset in response to any instructions of said first subset of instructions; and

fourth means coupled to said first means and to said second communication means for using said second communication means to indicate a status of said first means while said first means is executing instructions of said first subset.

10. A data processing system according to claim 8 further comprising:

mode switch means for switching between said first and second subsets of said instructions, said mode switch means being responsive to an externally-provided signal to switch from said first subset to said second subset; and

control means for disabling said mode switch means from switching to said second subset of said instructions.

13. A data processor comprising:

execution means for sequentially executing a plurality of instructions, said execution means having a first mode in which instructions of a first subset are executed and a second mode in which instructions of a second subset are executed;

communication means for providing said plurality of instructions to said execution means, said communication means operating in a master mode while providing instructions of said first subset and in a slave mode while providing instructions of said second subset, said communication means is coupled to a first plurality of pins and to a second plurality of pins, said communication means uses the first plurality of pins while providing instructions of the first subset and uses the second plurality of pins while providing instructions of the second subset, each of the second plurality of pins is either not used or is used only for development support functions while the communication means is providing instructions of the first subset;

mode switch means for switching between said first mode and said second mode and for preventing said communication means from operating in said slave mode while said execution means is executing instructions of said first subset.

14. A data processor according to claim 13 wherein said communication means further comprises:

controller means for operating a parallel communication bus as a bus master; and

a slave-only serial communication interface.

17. A data processor according to claim 13 wherein:

said mode switch means is responsive to an externally-provided signal to switch from said first mode to said second mode.

20. A data processor according to claim 13 further comprising:

control means for disabling said mode switch means from switching to said second mode of operation.

EXHIBIT A

claims, no construction is needed, citing *IMS Technology* Ltd. v. Samsung Electronics Co. Ltd., 215 F.3d 1281 (Fed.Cir.2000). Motorola proposes its construction in the event the Court determines that a construction is needed. The Court will construe the phrases at this phase of the present case.

ADI argues that the Vaglica patent plainly speaks to a single chip processor and that the disputed phrases

should be construed in the context of the patent. However, ADI points to nothing in the patent specification that plainly evidences an intent to alter the plain meaning of the phrases "data processor" and "data processing system" or to redefine those terms in any way. On the contrary, the Vaglica patent specification refers to "data processing systems" which have been constructed "as single integrated circuits, or even as a combination of a few such integrated circuits," acknowledging that a "data processor" or a "data processing system" may comprise a combination of integrated circuits. Vaglica patent, 1:24-27. ADI also points to nothing in the prosecution history that evidences a clear disavowal of the plain meaning of the phrases.

Motorola offers a dictionary definition for the term "data processor" taken from the IEEE Standard Glossary of Computer Hardware Terminology 620.20 (1994) and from the 2000 IEEE Dictionary. The two sources each define a "data processor" to be "a processor capable of performing operations on data. For example: a desk calculator or tabulating machine, or a computer." Motorola's proposed construction differs from this dictionary definition without explanation. The two sources cited by Motorola post-date the issuance of the Vaglica patent by two years and eight years, respectively.

The IEEE Standard Computer Dictionary 610 (C) 1990 and published January 18, 1991, has the following definitions:

data processing (DP)-"The systematic performance of operations upon data, such as data manipulation, merging, sorting, and computing."

data processing system-"A system including computer systems and associated personnel, that performs input processing, storage, output and control functions, to accomplish a sequence of operations or data."

Since the technical dictionary was published shortly before the patent was issued, the Court gives it more weight than the references cited by Motorola.

The Court will construe these disputed claims as follows:

"data processor" and **"data processing system"** means: a processor capable of systematic operations on data, such as data manipulation, merging, sorting, and computing.

"instructions"-claims 8, 13

There are several disputed phrases that involve the term "instructions," and the Court will treat those phrases together. The parties have not disputed the meaning of the term "instructions" itself for purposes of the Vaglica patent.

The phrase "plurality of instructions" is disputed. Motorola contends that the phrase means "two or more instructions," and ADI contends the phrase means "the full instruction set comprising all of the instructions that the data processor is capable of executing." The patent specifications and file history contain no evidence to support ADI's proposed construction. In standard dictionaries "plurality" when used in a claim, refers to two or more items, absent some indication to the contrary." Dayco Products, Inc. v. Total Containment, Inc. 258 F.3d 1317, 1327-28 (Fed.Cir.2001). The Court will construe the disputed phrase as follows:

"plurality of instructions" means: two or more instructions.

"first subset of said instructions"

Motorola contends the ordinary meaning of the phrase "first subset of said instructions" is a "first subset of a plurality of instructions," and that ordinary meaning should govern. ADI argues that the phrase should be construed to mean "the instruction set that the data processor can execute in the normal execution mode." The references to the patent specification cited by ADI do not dictate the construction offered by ADI. The Court will construe the phrase **"first subset of said instructions"** according to its ordinary meaning to be "a first subset of the plurality of instructions referenced earlier in the claim."

"second subset of said instructions"

Again, Motorola argues that the ordinary meaning of the term "second subset of said instructions" should apply, namely, "a second subset of the plurality of instructions." ADI argues the phrase should be interpreted to mean "distinct from the first subset of instructions, the instruction set that the data processor can execute in the debug mode; includes one or more special debugging instructions." Again, the citations to the specification upon which ADI relies do not dictate the construction offered by ADI. However, unless the "second subset" is different from the first, it is a meaningless term. The Court will construe the disputed phrase as follows:

"second subset of said instructions" means: a second subset of the plurality of instructions referenced earlier in the claim, which is not exactly the same as the first subset.

The parties dispute the phrases **"first subset of said plurality of instructions"** and **"second subset of said plurality of instructions,"** making the same arguments mentioned above. For the reasons stated, the Court will construe the phrase **"first subset of said plurality of instructions"** to mean "a first subset of the plurality of instructions referenced earlier in the claim." The Court will construe the phrase **"second subset of said plurality of instructions"** to mean "a second subset of the plurality of instructions referenced earlier in the claim which is not exactly the same as the first subset."

Two additional phrases-**"instructions of said first subset"** and **"instructions of said second subset"**-are also disputed. Motorola and ADI offer the same constructions for these terms as they offered for "first subset of said instructions" and "second subset of said instructions," respectively, although the phrases are different. For the reasons stated, the Court will construe the phrase **"instructions of said first subset"** to mean "instructions that are members of the first subset of the plurality of instructions." The Court will construe the phrase **"instructions of said second subset"** to mean "instructions which are members of the second subset of the plurality of instructions which is not exactly the same as the first subset."

"first means for executing said instructions"-claim 8 & 13

The parties agree this claim element, found in claims 8 and 13, is in "means plus function" form and should be construed under 35 U.S.C. s. 112, para. 6. The recited function for this claim element is "for executing said instructions," and the parties do not dispute that function or its meaning. Motorola proposes that the structure disclosed in the specification for performing the recited function is the CPU 11, shown in Figure 1. ADI contends that the corresponding structure is a collection of certain of the components of the CPU 11, but not the CPU 11 in its entirety. In particular, ADI contends that the "first means" structure disclosed in the specification is execution unit 20 (Figure 3), execution unit 52 (Figure 4), IR pipe 23 (Figure 3), IR pipe 51, sequencer 53 and microcode 54 (Figure 4). Each of the parties cites to certain excerpts from the patent

specification.

The dispute between the parties is whether the entire CPU should be regarded as the "execution means," or whether only specific portions of the CPU are involved in performing the recited function. While the patent specification does suggest in general terms that the CPU 11 executes instructions (see Vaglica patent, 8:36-38), in other places, the specification is more specific in stating that the execution unit 20, a portion of the CPU 11, actually performs the function of executing instructions. For example, the specification states that instructions are "executed by execution unit 20." Vaglica patent, 8:39-41. The specification also states that "execution unit 20 contains all of the arithmetic, shift, register and other logic necessary to execute each of the normal and special debug instructions of CPU 11." Vaglica patent, 7:51-53. Each instruction passes through (TR) Pipe 23 prior to and **while** it is actually being executed. Vaglica patent 7 :47-50. (emphasis added) Other portions of the CPU perform other functions and may be affected by the execution of instructions, but they do not themselves perform the function of executing the instructions. See, for example, 7:31-33, where the specification indicates that registers "are affected by normal program execution"; 8:9-12, where the specification indicates that "bus controller 40 ... operates IMB 12 as a bus master to fetch normal instructions and to read and write data." The sequencer 53 and the microcode 54 affect the execution unit, but they do not themselves execute the instructions. The Court will construe this disputed phrase as follows:

"first means for executing said instructions" is construed as execution unit 20 (Figure 3), execution unit 52 (Figure 4), instruction register pipe 23 (Figure 3), instruction register pipe 51 (Figure 4) and equivalents thereof.

"execution means for sequentially executing a plurality of instructions, said execution means having a first mode in which instructions of a first subset are executed and a second mode in which instructions of a second subset are executed

This phrase is found in claim 13 of the Vaglica patent, and the parties each propose the same construction for this phrase they proposed for the "first means" phrase discussed above.

The "execution means" element in claim 13 differs from the "first means" element of claim 8 in that the "execution means" of claim 13 is specified as "having a first mode in which instructions of a first subset are executed and a second mode in which instructions of a second subset are executed." Claim 8 does not specify that the "first means" has a "first mode" and "second mode."

The specification indicates generally that the CPU 11 executes instructions and, more specifically, that execution unit 20 "contains all of the arithmetic, shift, register and other logic necessary to execute each of the normal and special debug instructions of CPU 11." Vaglica patent, 7:24-26 and 51-53. However, only the CPU 11 is indicated as having two modes of operation-a normal mode and a debug mode. See, *e.g.*, 3:15-16, 8:55-61, 10:38-39 and 11:24-25. The specification states that the execution unit itself executes normal and debug instructions, but it does not indicate that the execution unit executes those instructions using two modes of operation.

Since the CPU 11 is the structure disclosed in the patent specification which both executes instructions and has first and second modes of operation, the Court will construe the **"execution means"** element of claim 13 to be the CPU 11 and equivalents thereof.

"second communication means"-claim 8

The parties agree that this element of claim 8 is in "means plus function" form. The dispute surrounding the construction of this element goes to whether the patent specification discloses a structure for performing the recited function. ADI contends that the specification fails to describe a specific structure, but ADI agrees that if the Court finds sufficient structure is disclosed for the recited function, that structure is as proposed by Motorola.

The function recited in claim 8 for the "second communication means" is "for providing instructions of said second subset to said first means." The claim includes additional limitations on the "second communication means," requiring it to be "distinct from said first communication means" and requiring it to be "not operative for communication of instructions of said second subset in response to any instructions of said first subset of instructions."

ADI argues that the requirement that the second communication means "is not operative ...." is an additional function to be performed by the "second communication means." Although the quoted language describes a characteristic of the "second communication means," it does not set forth an additional function to be performed by the "second communication means."

The patent specification states:

"The background debug mode of operation involves toggling CPU 11 into a mode in which execution of normal instructions fetched via IMB 12 is halted and execution proceeds with special debugging instructions which are received by means of a serial communication interface comprising the IPIPE/DSO, IFETCH/DSI and BKPT/DSCLK pins."

Vaglica patent, 3:27-33. Thus, at least the IPIPE/DSO, IFETCH/DSI and BKPT/DSCLK pins perform the function of providing instructions of the second set (for example, debug instructions) to the "first means." These pins are shown in Figures 1 and 4 of the Vaglica patent. The patent specification describes sufficiently specific structure for performing the function recited in claim 8 for the "second communication means."

The Court will construe the **"second communication means"** element of claim 8, as agreed by the parties, to include the background mode serial logic 45, serial interface 55, and pins IPIPE/DSO, IFETCH/DSI and BKPT/DSCLK, and equivalents thereof.

"mode switch means"-claim 10

Claim 10 calls for a "mode switch means for switching between said first and second subsets of said instructions, said mode switch means being responsive to an externally-provided signal to switch from said first subset to said second subset." The parties agree this claim element is in "means plus function" form and should be construed according to 35 U.S.C. s. 112, para. 6. The parties also agreed in the Joint Claim Construction Statement as to what the corresponding structure is for the "mode switch means," namely, "structure responsive to BKPT, to background instruction, or to double bus faults; logic for asserting FREEZE signal; and instruction to resume normal mode."

ADI contends the patent specification fails to describe any structure for performing the function, rendering the limitation indefinite. Motorola disagrees, arguing that "the patent explicitly describes in detail 'three

different methods for entry into the background debug mode'-that is, for switching modes." ADI responds by pointing out that "methods" are not the same as "structure."

In its letter to the Court dated January 28, 2004, Motorola proposed greater specificity in the structure for this element. As the Court understands, Motorola is proposing that the data processor switches from the first mode of operation to the second mode of operation when, either, a device connected to the IMB 12 transmits a BKPT signal to the bus controller 50, an external device transmits a BKPT signal to the bus controller 50, the CPU fetches background instructions from the memory, or the occurrence of double bus faults; and then the CPU transmits a FREEZE signal via the IMB to other devices on the IMB. Motorola also proposes that the data processor switches from the second mode to the first mode when the external device transmits an instruction to the CPU via the DSI line.

The function recited for the "mode switch means" is "for switching between said first and second subsets of said instructions." The "mode switch means" must also "be[ing] responsive to an externally-provided signal to switch from said first subset to said second subset." The patent specification describes several events that can cause the processor to enter a debug mode. Those events include assertion of a BKPT signal, the execution of a background instruction, or to double bus faults. Vaglica patent, 10:17-25. According to the specification, the BKPT signal is an input to bus controller 50, seen in Figure 4, and that signal may be received by the bus controller 50 by way of the BKPT signal line of IMB 12 or the direct BKPT input to CPU 11, providing a "hardware" breakpoint. Vaglica patent, 9:24-26; 9:39-41; 10:17-21. The BKPT signal is shown as an input signal to the CPU 11, and the bus controller 50 is a part of the CPU 11. Vaglica patent, 4:53-54; Fig. 4. The specification also states that a "software" breakpoint "simply comprises one or more of the normal instructions which are responded to as breakpoint instructions." Vaglica patent, 9:43-47. When the CPU 11 enters the background debug mode, it asserts the FREEZE signal on the IMB 12. The FREEZE signal is shown as an output signal from the CPU11. Vaglica patent, 4:54-56. The CPU 11 may be made to re-enter its normal mode of operation by means of an instruction included in the set of debug instructions. Vaglica patent, 12:1-9.

Thus, the bus controller 50 the CPU 11 are structures that perform the function of switching from the first subset of instructions to the second subset of instructions. The CPU 11 performs the function of switching from the second subset of instructions to the first subset of instructions. The bus controller 50 is responsive to an externally-provided signal to switch from the first subset to the second subset.

Accordingly, the Court will construe the **"mode switch means"** element of claim 10 to be the CPU 11, including the bus controller 50, and equivalents.

"externally-provided signal"-claim 10

Although this claim term was initially disputed, after the Markman hearing, the parties reached agreement on its construction. The parties agree this term should be construed as "a signal provided from outside the data processor." Letter dated January 28, 2004 from Motorola counsel; letter dated February 6, 2004 from ADI counsel.

"master mode"

Motorola proposes that the "master mode" refers to "a mode in which a first subset of the plurality of instructions is provided to the execution means while operating under control of the CPU," citing to Vaglica patent, 8:56-61. ADI proposes the term should be construed to mean "operating under the control of the

central processing unit of the data processor acting autonomously," citing to Vaglica patent, 8:53-61 and 10:38-65. Neither party relies on a dictionary source.

In a letter to the Court dated February 6, 2004, ADI modified its proposed construction to be "the central processing unit of the data processor acting independently from the external development system." Motorola responded in its letter of February 11, 2004 that ADI's modified proposed construction excludes the preferred embodiment described in the specification, arguing that the preferred embodiment does not require the CPU to operate independently or autonomously. Motorola argues that, during the "master mode," the CPU can communicate with the external development system.

Referring to Figure 4 of the patent, the specification states that:

In the normal mode of operation, a bus controller 50 fetches instructions and data operands from memory by means of a data bus and an address bus (which are merely the data and address portions of IMB 12 of Fig. 1), which are operated by bus controller 50 as a bus master. Instructions are passed from bus controller 50 to IR pipe 51 and data operands are passed to an execution unit 52.

Vaglica patent, 8:55-63. The specification goes on to state:

Once debug mode is entered, interrupts to CPU 11 are not acknowledged or acted upon and instruction tracing is disabled. Debug instructions and any address and/or operand data required for the execution thereof are provided to IR pipe 51 by serial interface 55. Serial interface 55 receives these instructions and data from an external development system via the DSI pin.... Since DSCLK is provided by the external development system, it controls the serial interface and is said to be the master thereof. Serial interface 55 operates as a slave.

Vaglica patent, 10:40-55.

Elsewhere, in connection with Figure 3, the specification states that "an output of micro ROM 34 is coupled to bus controller 40, which operates IMB 12 as a bus master to fetch normal instructions and to read and write data." Vaglica patent, 8:9-12.

During prosecution of the Vaglica patent, the Applicant argued that the specification "describes the operation of a bus controller 50 as a bus master while the apparatus is in its normal mode." The Applicant went on to argue "a first communication means (bus controller 50) and a second communication means (serial interface 55) ... operate in master and slave modes, respectively." Amendment of May 2, 1989, pp. 6,7.

In one mode of operation of the CPU, the bus controller 40/50 functions as a "master" to operate the bus 12 to fetch normal instructions and to read and write data. The bus controller 40/50 provides instructions to the IR pipe 23/51. In a second mode of operation of the CPU, the serial interface 55 operates as a "slave" under control of an external development system. Thus, in the "master mode," the bus controller controls the fetching of instructions and providing those instructions to the IR pipe and, thus, to the execution unit. In the "slave mode," the serial interface, under control of the external development system, provides instructions to the IR pipe and, thus, to the execution unit. In the "master mode," the providing of instructions is controlled by the bus controller, a device internal to the data processor, whereas in the "slave mode," the providing of instructions via the serial interface is controlled by the development system, a

device external to the data processor. The court will construe this disputed term as follows:

"master mode" means: a mode in which the providing of instructions is controlled by a device internal to the CPU.

"bus master"-claims 14, 22, & 27

This phrase appears in claims 14, 22 and 27 of the Vaglica patent. Motorola proposes a construction of "the bus while under the control of the CPU." ADI proposes a construction of "operating the bus under the control of the central processing unit of the data processor acting autonomously."

The Court finds that the term "bus master" does not refer to the bus itself, but rather it refers to a device that controls the bus. As mentioned above, the specification describes the bus controller as acting "as a bus master" in the normal mode of operation. For the reasons set out above in connection with the term "master mode," the Court will construe this disputed term as follows:

"bus master" means: a device that controls the bus, such as a bus controller.

"slave mode" / "slave-only"-claims 13 and 14

The parties agree that the phrase "slave-only" in claim 14 means "operating only under the control of a system external to the data processor." Motorola's Opening Brief, Exhibit 5G. The parties also agree that the phrase "slave mode" in claim 13 involves operating "under the control of a system external to the data processor." The parties differ in their proposed construction of "slave mode" only in that Motorola argues that the "slave mode" is "a mode in which a second subset of the plurality of instructions is provided to the execution means."

Claim 13 specifically recites that the "communication means" operates in a "slave mode while providing instructions of said second subset" to the "execution means." Because that requirement is set out in the claim itself, it need not be included in the definition of the phrase "slave mode." The Court will construe these disputed phrases as follows:

"slave mode" / "slave-only" mean: operating under the control of a system external to the data processor.

"pins/first and second plurality of pins"-claim 13

The term "pins" is found in claims 13, 22, 24 and 25 of the Vaglica patent (claims 22, 24 and 25 are no longer asserted by Motorola). Motorola argues the term should be construed as "electrical connections between two components," citing to the McGraw-Hill Dictionary of Scientific and Technical Terms (4th ed., 1989) for the definitions of "pin" and "terminal." ADI argues the term "pin" should be construed as "the external leads of an integrated circuit package for electrical connection to external devices," citing The American Heritage Dictionary of the English Language (4th ed., 2000). The primary dispute between the parties appears to be whether the "pins" must be "external."

The McGraw-Hill Dictionary of Scientific and Technical Terms defines "pin" to be "a terminal on an electron tube, semiconductor, integrated circuit, plug, or connector. Also known as base pin; prong," and it defines "terminal" as "a screw, soldering lug, or other point to which electrical connections can be made." The American Heritage Dictionary cited by ADI defines "pin" as "Electronics: a lead on a device that plugs

into a socket to connect the device to a system." The specification of the Vaglica patent uses the term "pins" to consistently refer to leads on the microcomputer 10 that provide for connection to devices external to the microcomputer 10. See Vaglicapatent, 2:55-58; 2:60-62; 2:67-3:16; 3:27-33; 3:41-43; 6:9-ll; 6:26-30; 10:10-11; 10:17-25; Fig. 1. Elsewhere, the specification describes "connections" between components within the microcomputer 10. See Vaglica patent, 2:67-3:2; 7:43-45; 10:17-25.

While a "pin" is a point of "connection," the Court finds that the term "pin" denotes a particular type of connection point. In other words, while all "pins" may be points of connection, not all points of connection would be "pins." The cited dictionary definitions suggest that a "pin" is more than simply an "electrical connection," rather, a "pin" is something to which electrical connections may be made. The patent specification consistently uses the term "pin" to refer to a lead external to the microcomputer 10 that facilitates connection to devices external to the microcomputer 10. For example, see 6:9-11. The microcomputer 10, according to the specification, is "an integrated circuit data processing system." Vaglica patent, 2:45-51. Thus, the "pins" facilitate connection to devices external to the exemplary integrated circuit data processing system. Some of these "pins" are used to connect the data processing system to a development system external to the data processing system (3:2-16), and others are used to connect the data processing system to external devices and systems (2:55-58). The Court found no instance of the specification using the term "pin" to describe any connection internal to the data processing system. Rather, the specification repeatedly refers to "external" devices and systems, referring to devices and systems outside the data processing system. Also, in connection with the phrase "externally-provided signal," the parties have agreed that this signal, which in the embodiment described in the specification is the BKPT signal, is provided "from outside the data processor." The court will construe these disputed phrases as follows:

"pin" means: a terminal or point at which devices or systems external to the data processing system may be connected to the data processing system,

"first plurality of pins" means: a first group of two or more pins,

"second plurality of pins" means: a second group of two or more pins.

"development support function"-claims 1, 13, & 22

This phrase is found in claims 1,13 and 22 of the Vaglica patent, but claims 1 and 22 are no longer asserted. Motorola proposes the phrase be construed as "functions used for designing, verifying, testing, and observing the operation of (*i.e.,* 'debugging') a program or the data processor." ADI proposes the phrase be construed as "for special functions used for debugging during the design and development stage of a data processor product."

Motorola cites to the specification, at 1:16-23 which states:

"Development systems are used in conjunction with data processing systems to assist in the 'debugging' of both hardware and software. Typical functions of development systems include the insertion of and response to breakpoints, halting the execution of the data processor to examine and perhaps alter the contents of various system registers and the like and tracing the execution of software."

The specification also indicates that:

"The development support features of microcomputer 10 include: a 'background debug' mode of operation, trackability of the instruction pipeline of CPU 11, external visibility of IMB bus cycles and the ability both on-board modules and external devices to insert breakpoints."

Vaglica patent, 3:21-26.

From the specification, it is clear that "development support functions" are not limited to data processors, but may apply to both hardware and software. The specification does not indicate that these functions apply only during the design and development of a data processor product. However, as ADI points out, "observing the operation" of a program might apply to the normal operation of a program as observed by a user. The Court will construe this phrase as follows:

"development support functions" means functions used for designing, verifying, testing, and debugging a program or the data processor.

"mode switch means for switching between said first mode and said second mode and for preventing said communication means from operating in said slave mode while said execution means is executing instructions of said first subset"-claim 13

This phrase is found in claim 13 of the Vaglica patent, and the parties agree it is in "means plus function" form, subject to construction according to 35 U.S.C. s. 112, para. 6. Motorola proposes that the structure from the specification that performs the recited functions is "structure responsive to BKPT (in bus controller 50), to background instruction, or to double bus faults; and logic that asserts the FREEZE signal; and instruction to resume normal mode; and equivalents." ADI asserts the specification fails to disclose any structure for performing the recited functions, rendering the claim element indefinite. ADI agrees that, if the Court finds the element to be definite, the corresponding structure is as proposed by Motorola.

In its letter to the Court dated January 28, 2004, Motorola proposed greater specificity in the structure for this element. As the Court understands, Motorola is proposing that the data processor switches from the first mode of operation to the second mode of operation when, either, a device connected to the IMB 12 transmits a BKPT signal to the bus controller 50, an external device transmits a BKPT signal to the bus controller 50, the CPU fetches background instructions from the memory, or the occurrence of double bus faults; and then the CPU transmits a FREEZE signal via the IMB to other devices on the IMB. Motorola also proposes that the data processor switches from the second mode to the first mode when the external device transmits an instruction to the CPU via the DSI line.

The "mode switch means" in claim 13 is similar to the "mode switch means" in claim 10, but the claim 13 element performs two functions-"for switching between said first mode and said second mode" and "for preventing said communication means from operating in said slave mode while said execution means is executing instructions of said first subset." The first recited function is the same as that function performed by the "mode switch means" in claim 10. The second recited function is very similar to that function performed by the "control means" in claim 10.

For the reasons set forth above in connection with the "mode switch means" of claim 10 the Court will include within the structure of the claim 13 "mode switch means" the CPU 11, including the bus controller 50. The parties agreed that the structure of the "control means" element of claim 10 is a latch for latching the

state of the BKPT pin, and accordingly, the Court will also include within the "mode switch means" of claim 13 the latch for latching the state of the BKPT pin. Therefore, the **"mode switch means"** of claim 13 will be construed as the CPU 11, including the bus controller 50, and the latch for latching the state of the BKPT pin, and equivalents of that combination.

"first and second modes"-claim 13

The phrases "first mode" and "second mode" are found in claim 13 of the Vaglica patent. The parties each cite to the specification for support, with Motorola proposing the phrases mean "first and second modes of operation: the ability to receive instructions from two sources," and ADI proposing the phrases mean "distinct operating states of the data processor: the first mode is a normal execution mode and the second mode is a debugging mode."

The term "mode" means simply a manner or way of doing, acting or operating. The specification uses the term consistently with this ordinary meaning, and the prosecution history does not suggest any special meaning. The Court will construe these terms as follows:

"first mode" means a first manner or way of operating, and

"second mode" means a second manner or way of operating.

"slave-only serial communication interface"-claim 14

This phrase is found in claim 14. The parties have agreed that "serial communication interface" is "a communication interface in which data is transferred one bit at a time." The parties have also agreed that the phrase "slave-only" means "operating only under the control of a system external to the data processor."

The Court will construe the phrase **"slave-only serial communication interface"** to mean a communication interface, operating only under the control of a system external to the data processor, in which data is transferred one bit at a time.

"said mode switch means is responsive to an externally-provided signal to switch from said first mode to said second mode"-claim 13

This phrase is found in claim 17, which depends from claim 13. A very similar phrase is found in claim 10. The parties dispute whether this phrase is in "means plus function" form. The Court finds that this phrase defines an additional limitation on the "mode switch means" element set out in claim 13. This additional limitation is not a "means plus function" limitation, nor is it adding another function to the "mode switch means." As in the case of the "responsive to" language in the "mode switch means" element of claim 10, this language describes an additional characteristic of the "mode switch means." The parties have agreed to the meaning of the phrase "externally-provided signal," and the Court has construed the terms "first mode" and "second mode." The Court finds that no additional construction is needed for this phrase.

CONCLUSION

The jury should be instructed in accordance with the court's interpretation of the disputed claim terms in the Vaglica patent.

Signed June *16,* 2004.

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