United States District Court,
E.D. Texas, Beaumont Division.

MOTOROLA, INC,
v.
ANALOG DEVICES, INC.

No. 1:03-CV-131

March 23, 2004.

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MEMORANDUM OPINION AND ORDER CONSTRUING CERTAIN CLAIMS OF UNITED STATES PATENT NO. 4,279,947 **(GOLDMAN), NO. 4,446,194 (CANDALERIA), NO. 5,026,667 (ROBERTS), NO. 5,479,084 (YALLUP), AND NO. 5,040,144 (PELLEY)**

RON CLARK**, District Judge.**

Plaintiff, Motorola, Inc. ("Motorola"), filed suit claiming infringement of five patents by Analog Devices, Inc. ("A.D.I."). A .D.I. counter-claimed alleging infringement by Motorola of six other patents. All of the patents involve various aspects of microchip production, manufacture, programming, or design. On January 21, 2003, the court conducted a hearing for the purpose of hearing evidence and argument that would assist the court in interpreting the meaning of certain disputed claims of United States Patent No. 4,279,947 (the "959 patent" or "the Goldman patent"), United States Patent No. 4,446,194 (the "194 patent" or "the Candaleria patent"), United States Patent No. 5,026,667 (the "667 patent" or "the Roberts patent"), United States Patent No. 5,479,048 (the "048 patent" or "the Yallup patent") and United States Patent No. 5,040,144 ("the 144 patent" or "the Pelley patent"). Having carefully considered the parties' briefs, the testimony, and exhibits admitted into evidence, the referenced patents, and the arguments of counsel, the court now makes the following findings and construes the disputed terms as follows.

STANDARD FOR CONSTRUING CLAIM TERMS

In Markman v. Westview Instruments, Inc., 52 F.3d 967 (Fed.Cir.1995) ("*Markman I*"), the Federal Circuit held that claim construction is a matter of law. In affirming this decision, the Supreme Court in Markman v.

Westview Instruments, Inc., 517 U.S. 370, 116 S.Ct. 1384, 134 L.Ed.2d 577 (1996) ("*Markman II*"), stated, "[W]e hold that the construction of a patent, including terms of art within its claims, is exclusively within the province of the court," Id. at 1387, and "... judges, not juries, are the better suited to find the acquired meaning of patent terms." Id. at 1395.

The duty of the trial judge is to determine the meaning of the claims at issue, and to instruct the jury accordingly. In the exercise of that duty, the trial judge has an independent obligation to determine the meaning of the claims, notwithstanding the views asserted by the adversary parties. (citations omitted)

Exxon Chemical Patents, Inc. v. Lubrizoil Corp., 64 F.3d 1553, 1555 (Fed.Cir.1995).

In performing this duty, this court is guided by several principles. The claims should be construed in light of the ordinary meaning of the claim language, as well as the patent specification and prosecution history. Markman I, 52 F.3d at 979-80; *see also* Vitronics Corp. v. Conceptronic, Inc. 90 F.3d 1576, 1582 (Fed.Cir.1996).

The court should first determine the ordinary meaning of a disputed term. There is a "heavy presumption" that the terms used in claims "mean what they say and have the ordinary meaning that would be attributed to those words by persons skilled in the relevant art." Tex. Digital Sys., Inc. v. Telegenix, Inc., 308 F.3d 1193 (Fed.Cir.2002).

It is well established that courts are to determine the plain, ordinary meaning of a claim term *before* turning to the specification. As the Federal Circuit has stated:

... consulting the written description and prosecution history as a threshold step in the claim construction process, *before* any effort is made to discern the ordinary and customer meanings attributed to the words themselves, invites a violation of our precedent counseling against importing limitations into the claims." Tex. Digital, 308 F.3d at 1204 (emphasis supplied).

It is entirely appropriate for a court to look to dictionaries to determine the plain and ordinary meaning of a disputed claim term. *Id*. at 1202.

A dictionary is not prohibited extrinsic evidence, and is an available resource of claim construction. Although a dictionary definition may not enlarge the scope of a term when the specification and the prosecution history show that the inventor, or recognized usage in the field of the invention, have given the term a limited or specialized meaning, a dictionary is often useful to aid the court in determining the correct meaning to be ascribed to a term as it was used.

Vanguard Products Corp. v. Parker Hannifin Corp., 234 F.3d 1370, 1372 (Fed.Cir.2000).

Then, the court should look to the intrinsic evidence of record, that is, the patent specification, and, if in evidence, the prosecution history, to determine whether the patentee clearly intended a meaning different from the ordinary meaning or whether he clearly disavowed the ordinary meaning in favor of some special meaning. *See* Markman I, 52 F.3d at 979.

Claim terms take on their ordinary and accustomed meanings unless the patentee demonstrated a "clear intent" to deviate from the ordinary and accustomed meaning of a claim term by redefining the term in the

patent specification. Johnson Worldwide Assoc., Inc. v. Zebco Corp., 175 F.3d 985 (Fed.Cir.1999).

Claims must be read in view of the specification, of which they are a part. Autogiro 384 F.2d at 397, 155 USPQ at 702; *see* Winans v. Denmead, 56 U.S. (15 How.) at 338; *Bates v. Coe,* 98 U.S. at 38-39. The specification contains a written description of the invention that must enable one of ordinary skill in the art to make and use the invention. For claim construction purposes, the description may act as a sort of dictionary, which explains the invention and may define terms used in the claims.

Markman I, 52 F.3d at 979.

The Federal Circuit offered guidance on how the written description can be helpful in determining the meaning of claims in Scimed Life Systems v. Advanced Cardiovascular, 242 F.3d 1337 (Fed.Cir.2001).

While it is true, of course, that "the claims define the scope of the right to exclude" and that "the claim construction inquiry, therefore, begins and ends in all cases with the actual words of the claim," Renishaw PLC, 158 F.3d at 1248, 48 USPQ 2d at 1121, the written description can provide guidance as to the meaning of the claims, thereby dictating the manner in which the claims are to be construed, even if the guidance is not provided in explicit definitional format.

The patentee may also deviate from the plain and ordinary meaning by characterizing the invention in the prosecution history using words or expressions of manifest exclusion or restriction, representing a "clear disavowal" of claim scope. Teleflex, Inc. v. Ficosa N. Am. Corp., 299 F.3d 1313, 1327 (Fed.Cir.2002). However, absent a "clear indication" from the patent specification or a "clear disavowal" in the prosecution history, there is a "heavy presumption" that a claim term is given its plain and ordinary meaning. Tex. Digital, 308 F.3d at 1202.

Extrinsic evidence may be considered if needed to assist in determining the meaning or scope of technical terms in the specification or claims to one of ordinary skill in the art. *Vitronics* at 1583.

THE GOLDMAN PATENT

U.S. Patent No. 4,279,947, the Goldman Patent, is held by Motorola and was issued on July 21, 1981. The Goldman Patent relates to a process for depositing a uniform layer of silicon nitride on wafers which are to be used in making semiconductor devices or "chips." The abstract in the patent describes the invention as follows:

Silicon nitride is pyrolytically deposited by the reaction of halosilane with ammonia in an evacuated system. The process is particularly useful in providing uniform layers of silicon nitride on silicon wafers to be used in the fabrication of semiconductor devices.

There are four claims-in-suit. Claim 1 is an independent claim, and Claims 2 through 4 are dependent from Claim 1.

Disputed Claim Terms of the Goldman Patent

Claim 1 is copied below with each disputed claim term printed in bold type.

1. A method for the pyrolytic deposition of silicon nitride upon a plurality of substrates which comprises

placing said plurality of substrates in a reactor tube **with their broad faces perpendicular to the flow of a mixture** of dichlorosilane and ammonia at a temperature of from **about 650 (deg.)C to about 1,000 (deg.)C** in a vacuum of **about 300 millitorr to about 10 Torr.**

Claim 1, Element 1-"with their broad faces perpendicular to the flow of a mixture."

Motorola argues that no construction is needed and that the ordinary meaning should be given to this phrase. A.D.I. proposes the phrase be interpreted to mean "the predominant flow of a mixture of gasses in the vicinity of the broad face of each substrate is perpendicular to the broad face of that substrate."

The plain meaning of this phrase indicates that the mixture of dichlorosilane and ammonia flows through the reactor tube, and the broad faces of the substrates are oriented perpendicular to that flow. The specification describes an embodiment in which wafers are placed in a reactor tube with their broad faces perpendicular to the long axis of the tube, and the flow of gases through the tube is generally along the long axis of the tube. The Goldman patent, Figs. 1 and 2; Col. 2,:25-29 and 38-43. Hence, the description in the specification is consistent with the plain meaning of the phrase. Nothing in the prosecution history of the Goldman patent suggests that the phrase is used to mean anything other than its plain meaning.

Moreover, claims 3 and 4 of the Goldman patent support the plain meaning. Specifically, claims 3 and 4 recite that the temperature is "ramped up ... along the direction of said flow." The patent specification states that "there can be a temperature variation along the tube, ... with the lowest temperature being near the gas inlet end of the tube and the highest temperature near the opposite end of the tube." The Goldman patent, Col. 2:62-67. Thus, "along the direction of said flow" in claims 3 and 4 refers to the general direction of flow through the reactor. Likewise, in claim 1, "the flow of a mixture" refers to the general direction of flow through the reactor.

A.D.I.'s proposed construction would appear to make the claim inconsistent with, and perhaps contradictory to, the specification. First, the claim does not specify that the broad faces be perpendicular to the flow "in the vicinity of each face," only that the broad faces be perpendicular to "the flow of a mixture." Moreover, in the embodiment described in the patent, the mixture of gasses enters one end of a reactor tube in which the wafers are placed, and it travels to an exhaust at the other end. In the described configuration, gas would likely *not* travel "in the vicinity of the broad face of each substrate" in a direction perpendicular to that broad face. Rather, when the gas enters one end of the reactor tube, it diffuses or travels in the manner of a cloud or flow along the length of the reactor tube.

Therefore, the Court interprets this claim phrase as follows:

"with their broad faces perpendicular to the flow of a mixture" means: the general direction of flow of a mixture of gasses through the reactor is perpendicular to the broad faces of the substrates.

Claim 1, Element 2-from about 650 (deg.)C to about 1,000 (deg.)C

Analog contends that the use of the word "about" makes Claim 1 indefinite. The Court disagrees. Words of degree do not in themselves render a claim indefinite. Seattle Box Company v. Industrial Crat & Pack, Inc., 731 F.2d 818, 221 (Fed.Cir.1984). A person skilled in the art would understand that there is necessarily some degree of measurement error when one is measuring temperature inside a closed reactor tube.

On the other hand, Motorola's proposed construction that the temperature range is not crucial, and the term

should be defined as "at approximately 650 (deg.)C to approximately 1,000 (deg.)C is not well founded. First, Analog correctly points out that an earlier presented claim during prosecution, which was not approved, contained the phrase "at an elevated temperature." Motorola then submitted a claim to specifically recite "a temperature of from about 650 (deg.)C to about 1,000 (deg.)C." Also, the word "approximately" is not helpful in defining the word "about" in this context.

At the claims construction hearing, it appeared that the parties agreed there is some measurement error. However, there was insufficient evidence presented for the Court to determine the precise amount of error which would be expected from equipment constructed utilizing the technology at the time the patent was issued. Accordingly, the Court interprets this claim element as follows:

"from about 650 (deg.)C to about 1,000 (deg.)C" means: 650 (deg.)C, plus or minus some reasonable measurement error, to 1,000 (deg.)C plus or minus some reasonable measurement error. The term "reasonable measurement error" will depend upon the accuracy of temperature measuring devices available for use in a closed reactor system such as this, at the time the patent was issued.

Claim 1, Element 3-"about 300 millitorr to about 10 Torr"

Again Analog claims that the word "about" makes this claim phrase indefinite. For the reasons stated above, the Court disagrees. Again, Motorola argues that the numerical limitations on vacuum readings are not critical. But Motorola's position is belied by the prosecution history in that an earlier presented claim with the words "in a vacuum" was not approved. The application was approved after Claim 1 was modified to recite the specific pressure range of "about 300 millitorr to about 10 Torr."

For the same reasons discussed in reference to the dispute over the temperature range, the Court interprets this claim phrase as follows:

"about 300 millitorr to about 10 Torr" means: 300 millitorr, plus or minus some reasonable measurement error, to about 10 Torr, plus or minus some reasonable measurement error. The term "reasonable measurement error" will depend upon the accuracy of vacuum measuring devices available for use in a closed reactor system such as this, at the time the patent was issued.

Claim 2-"the method of Claim 1 where said temperature is from about 730 (deg.)C to about 770 (deg.)C."

Again, the main term in dispute here is "about." The parties make the same arguments as discussed previously. The construction of the Court will be consistent with its earlier interpretation.

"about 730 (deg.)C to about 770 (deg.)C" means: 730 (deg.)C, plus or minus some reasonable measurement error, to 770 (deg.)C, plus or minus some reasonable measurement error. The term "reasonable measurement error" will depend upon the accuracy of temperature measuring devices available for use in a closed reactor system such as this, at the time the patent was issued.

Claim 3-"the method of Claim 1 wherein the temperature is ramped up to about 100 (deg.)C along the direction of said flow."

A.D.I. argues that this claim phrase should be interpreted to mean that the temperature is increased from a lower temperature to 100 (deg.)C, plus or minus a measurement error of no more than 4 (deg.)C. In other

words, A.D.I. proposes that the highest allowable temperature in the reactor tube, under claim 3, would be about 100 (deg.)C. Motorola proposes that the phrase be interpreted to mean that a temperature gradient is established along the length of the reactor tube, wherein the temperature increases along the length of the tube so the temperature at the gas inlet of the tube is up to approximately 100 degrees Celsius lower than the temperature at the opposite end of the tube.

Phrases in a claim should be construed in the context of the claim as a whole. Claim 1, from which claim 3 depends, specifically requires a temperature range of about 650 (deg.)C to about 1,000 (deg.)C. Claim 2 recites a more limited temperature range of between 730 (deg.)C to about 770 (deg.)C. Given these temperature ranges, a construction of Claim 3 that the maximum temperature is ramped up only to about 100 (deg.)C, or the boiling point of water, would be internally inconsistent and nonsensical.

The parties agree that the term "ramped up" means "increased." Claim 3 indicates that the temperature increases "along the direction of said flow," referring to the flow of gasses through the reactor tube. This claim language, viewed in the context of the specification and the figures, makes it clear that the temperature throughout the tube will be in the range of about 650 (deg.)C to about 1,000 (deg.)C, as stated in Claim 1. The temperature will be increased by about 100 (deg.)C with the lower temperature being at the end of the tube where the gas enters and the higher temperature being at the end of the tube where the gas leaves the tube. The Goldman patent, Col. 2:61-67.

A.D.I. cites *Chef America, Inc. v. Lamb-Weston, Inc.,* 03-1279 (Fed.Cir. Feb. 20, 2004) in arguing that the plain meaning must be adopted, notwithstanding the result is nonsensical or inoperative. In *Chef America,* the Federal Circuit affirmed the district court's grant of summary judgment of non-infringement, based on a claim limitation requiring heating dough "to a temperature in the range of about 400 (deg.)F to 850 (deg.)F." Although the evidence was plain that heating the dough to such a temperature would render it completely unusable for its intended purpose, the Federal Circuit held:

These are ordinary, simply English words whose meaning is clear and unquestionable. There is no indication that their use in this particular conjunction changes their meaning.

The Court went on to say:

[W]here, as here, claims are susceptible to only one reasonable interpretation and that interpretation results in a nonsensical construction of the claim as a whole, the claim must be invalidated.... Where, as here, the claim is susceptible to only one reasonable construction, the canons of claim construction cited by [Chef America] are inapposite, and we must construe the claims based on the patentee's version of the claim as he himself drafted it.

The *Chef America* case is distinguishable from the present case. In *Chef America,* the district court found that "the specification supports the claim construction." The district court also found that "the prosecution history is also in accord with the construction that the temperature referred to is that of the dough," and that "the prior art is in accordance with construing the claims to require the dough be heated to a temperature in the range of 400 degrees to 850 degrees Fahrenheit." The Federal Circuit found that "[n]othing even remotely suggest that what is to be heated is not the dough but the air inside the oven in which the heating takes place."

In this case, there is ample evidence in the specification that the "ramp" is a temperature variation from

reactor inlet to reactor outlet. In fact, the specification contains nothing to suggest that the maximum temperature in the reactor will be 100 (deg.)C. Hence, unlike in *Chef America,* the specification clearly and unambiguously indicates that the temperature in the reactor varies from inlet to outlet by about 100 (deg.)C. Nothing in the specification or the prosecution history supports A.D.I.'s proposed construction.

The Court, therefore, interprets this claim phrase as follows:

"the temperature is ramped up to about 100 (deg.)C along the direction of said flow" means: The temperature in the reactor tube is increased along the length of the tube so that the temperature at the end of the tube where the gas exits is about 100 degrees Celsius higher than the temperature at the end of the tube where the gas enters.

Claim 4-"the method of Claim 1 wherein the temperature is ramped up from about 10 (deg.)C to 50 (deg.)C along the direction of said flow."

The parties make the same arguments about the term "ramped up" as they did for Claim 3. For the reasons discussed under Claim 3, the Court defines this claim term as follows:

"the temperature is ramped up from about 10 (deg.)C to 50 (deg.)C along the direction of said flow" means: The temperature in the reactor tube is increased along the length of the tube so that the temperature at the end of the tube where the gas exits is about 10 (deg.)C to about 50 (deg.)C higher than the temperature at the end of the tube where the gas enters.

THE CANDALERIA PATENT

U.S. Patent No. 4,446,194, the Candaleria Patent, is held by Motorola and was issued May 1, 1984. The Candaleria Patent teaches a method for avoiding the formation of voids in layers on a multi layer chip or electronic device, when the device is heated. The abstract in the patent describes the invention as follows:

When multilayer-metal electronic devices are heated, voids can form in the metal layers. Void formation is avoided by using a double die lectric layer as the interlayer die lectric. The double layer has a first oxide layer portion in contact with the first metal which is formed by plasma assisted chemical vapor deposition, and a second oxide layer portion formed by other means. The plasma formed oxide layer portion is believed to be in compressive stress relative to the substrate.

Disputed Claim Terms of the Candaleria Patent

The Candaleria patent has twelve different claims, but only four are claims-in-suit, namely claims 1 and 2, 4 and 5. Claims 2 and 5 are dependent claims from claims 1 and 4 respectively. The four claims are set out below, with the disputed terms in bold.

1. In a process for fabricating electronic devises where a **first metal layer** is formed on a first die lectric layer on a substrate, an **interlayer die lectric is formed on** said first metal layer, and a **second metal layer** is formed on said interlayer die lectric, the improvement comprising, forming said interlayer die lectric by depositing on said first metal layer a plasma derived **oxide** and overlying said plasma derived oxide with an **other oxide formed by other means.**

2. The process of claim 1 wherein said depositing step comprises depositing said plasma derived **oxide** by

plasma enhanced chemical vapor deposition and wherein said other oxide is **formed by chemical vapor deposition.**

4. In a process for fabricating electronic devices wherein a **first metal layer** is form on a first die lectric layer on a substrate, and **interlayer die lectric is formed on** said first metal layer, and a **second metal layer** is formed on said interlayer die lectric, the improvement comprising, forming said interlayer die lectric by depositing on said first metal layer a first **oxide** exhibiting intrinsic compressive stress relative to said substrate, and covering said first layer by a second layer not exhibiting substantial intrinsic compressive stress relative to said substrate and formed by a different process than said first oxide layer.

5. The process of claim 4 wherein said depositing step comprises depositing said first **oxide** by plasma enhanced chemical vapor deposition.

Claims 1 & 4, Element 1 "first metal layer"

The parties at first disagreed over this term in two respects, but at the hearing Motorola agreed with ADI's proposed construction that **first** in "first metal layer" means: "a metal layer formed before the second metal layer."

Motorola argues that the term "layer" is so widely used there can be no misunderstanding what it is or means. Analog disputes the meaning of "layer," stating that it should be defined as "a sheet or regular pattern formed by the same material." *Webster's Third New International Dictionary* defines "layer" as: "One thickness, course, or fold laid or lying over another ...," but there is no indication in the dictionary definition, in common usage, nor in the claims or specification that a layer must necessarily be "a sheet or regular pattern" or even consist entirely of the "same material." For example, the specification, at Col. 1:50-53, refers to an aluminum alloy being used for a metal layer. An alloy is a combination of materials. The same sentence indicates that "one of the several die lectric layers includes a nitride material." This implies that the layer might include materials other than a nitride material. The court recognizes the potential problems in using a non-scientific dictionary to define technical words, however, not every word in a patent is a "technical" word. In the context of this patent and these claims, and in view of the dirth of explanation from either party as to why "layer" should be given a special technical meaning, the court is faced with the choice between instructing a jury to interpret words that are not defined, by using their common, everyday meaning, or using a definition that fits the situation and properly explains the term, even though that definition is taken from a non-technical dictionary. The court chooses the latter course and for purposes of this patent, the court interprets this claim term as follows:

"layer" means: a uniform or varied thickness of a material or alloy laid or lying over or under another thickness of a material or alloy.

Claims 1, 4, Element 2-"interlayer die lectric"

Motorola proposes that this term means "a layer of electrical isolation material between metal layers." ADI's proposed construction is "a structure, formed by two layers of material, as recited in the claim, that provides electrical isolation between two metal layers." Thus, the parties argree that the "interlayer die lectric" provides electrical isolation between metal layers. The parties differ in that Motorola argues that the "interlayer die lectric" is "a layer," whereas A.D.I. argues that the "interlayer die lectric" is "a structure, formed by two layers of material, as recited in the claims."

Claim 1 specifically recites that the interlayer die lectric is formed by "depositing ... a plasma derived oxide and overlying" that oxide with "an other oxide formed by other means." Thus, the claim requires the interlayer die lectric to comprise two oxides. Motorola's proposed construction appears to imply that the interlayer die lectric may comprise a single "layer," and because of this court's definition of "layer" above, such an implication could lead to confusion in view of the additional recitations in the claim.

On the other hand, A.D.I. would define the term "interlayer die lectric" as limited to the two layers as further described in the claim. In other words, the modifying words in the claim describing the "interlayer die lectric" appear to be the definition ADI is proposing.

Plainly, from the claim, the interlayer die lectric comprises two layers, the first a plasma derived oxide and the second an oxide "formed by other means," discussed below. Thus, two oxide layers are required, but because the transitional phrase "comprising" is used, the interlayer die lectric is not limited to the two oxide layers. Neither the specification nor the prosecution history require that the interlayer die lectric be limited to only two oxide layers. The passages from the prosecution history on which A.D.I. relies do no constitute the "clear and unmistakable statements of disavowal" needed to limit the interlayer die lectric to only two layers. Cordis Corp. v. Medtronic AVE, Inc., 339 F.3d 1352, 1538 (Fed.Cir.2003). In setting out the background of the invention, the patent states that "the interlayer die lectric serves to passivatate the first metal layer as well as insulate and separate it from the overlying second metal layer." The Candaleria patent, Col. 1: 28-32. The court interprets this claim term as follows:

"interlayer dielectric" means: an insulating (non-conductive) structure of material(s) placed between two conductive layers.

Claims 1 & 4, Element 3-"formed on"

Motorola proposes that no construction is needed for this term and it should be given its "ordinary meaning." However, trial courts should set forth an express construction of material claim terms in dispute because the claim construction becomes the basis for jury instructions should the case go to trial. *See* AFG Industries, Inc. v. Cardinal IG Company, Inc., 239 F.3d 1239, 1247 (Fed.Cir.2001).

A.D.I. argues that "formed on" should be construed as "directly formed on." The dispute may be better understood by use of the analogy of paint on a wall. A.D.I. would argue that to be "formed on" the wall, the paint must be directly placed on the wall with no intervening layer of paint. A.D.I. cites in support two figures from the patent and certain descriptions from the specification. However, descriptions of preferred embodiments contained in the specifications should not be used to import limitations into the claims themselves. It is important to note that neither the claims nor the specification uses the words "directly formed on." *See* AFG Industries, Inc., 239 F.3d at 1251.

The ordinary usage of the phrase "formed on" would not be limited to "directly formed on, without any intervening material." Therefore, the court interprets **"formed on"** as follows:

a material (whether it is an interlayer die lectric or a metal layer) is **"formed on"** a layer when it is placed on and bonded to that layer or material, with or without the presence of an intervening material or layer.

Claims 1 & 4, Element 4-"second metal layer"

The parties agree that "first metal layer" would be "a metal layer that is formed before the second metal

layer." Therefore, a

"second metal layer" means: a metal layer that is formed after the first metal layer.

Claim 1, Element 5-"an other oxide formed by other means"

Motorola contends this phrase means "forming a second layer of die lectric oxide over the plasma derived oxide layer, wherein the second layer of oxide is formed by a process different from that used to deposit the underlying oxide." A.D.I. asserts that the use of the word "means" invokes a presumption that this is a means-plus-function claim element governed by 35 U.S.C. Section 112, Paragraph 6. Using this interpretation, A.D.I. seeks to limit the construction by defining the term as "overlying the plasma derived oxide with die lectric material using an ordinary chemical deposition process."

The word "means," together with a recital of function to be performed by the "means," may be used in a claim to designate an element of a structural combination. When the claim is directed to a method, as is claim 1 here, the phrase "step for," together with a recitation of a function to be performed, may designate an element of the claimed method. In each of those cases, a presumption is invoked that the claim element is to be construed according to 35 U.S.C. Section 112, Paragraph 6. However, in this case, the word "means" is not used to designate an element of a claimed combination. Accordingly, the Court finds that this is not a means-plus-function claim element, and 35 U.S.C. Section 112, Paragraph 6, does not apply.

The word "means" in claim 1 simply refers to a process or method by which an oxide may be formed. In particular, the claim simply requires that the "other oxide" be formed by a method other than "plasma derived." The prosecution history also makes clear that "different processes" are used to produce the two oxide layers. Amendment dated October 14, 1983, p. 6. However, nothing in the prosecution history indicates that, in claim 1, the "other oxide" must be formed by "an ordinary chemical vapor deposition process." Moreover, nothing in Claim 1, nor in the specification, indicates that the only other means for forming the "other oxide" must be "an ordinary chemical deposition process."

Claim 1 and the prosecution history make clear that the first layer of the interlayer die lectric is formed by a plasma derived oxide, for example, by a plasma assisted chemical vapor deposition (PACVD), sometimes referred to as a plasma enhanced chemical vapor deposition (PECVD) See Col. 7: 37-43. (The parties agreed in the Joint Claim Construction, page 13, that PECVD and PACVD are the same .) It is not proper to import limitations from the specification to the claim and to thereby limit the "other means" to an "ordinary" chemical vapor deposition process. The claim itself modifies "means" only by the word "other." Since the claim has already described a plasma derived oxide, which is formed by, for example, PACVD or PECVD, then the second layer must be formed of an oxide that is not plasma derived. The Court construes this claim term as follows:

overlying said plasma derived oxide with **"an other oxide formed by other means"** means: overlying the plasma derived oxide with an oxide that is not plasma derived.

Claim 2-"formed by chemical vapor deposition."

By a letter dated February 6, 2004, A.D.I. set out what it believes is now an agreed construction for the phrase "chemical vapor deposition." By a letter of February 11, 2004, Motorola has agreed with A.D.I. The agreed construction for "chemical vapor deposition" is "a conventional deposition process for applying a material to a substrate by thermal decomposition and reaction of gaseous source materials that is different

than plasma-enhanced chemical vapor deposition." This construction is consistent with the specification and prosecution history of the Candelaria patent.

THE ROBERTS PATENT

U.S. Patent No. 5,026,667, the Roberts Patent, is held by A.D.I. and was issued on June 25, 1991. It teaches a method of protecting integrated circuit chips from the stress imposed when the chips are "packaged" in plastic after they are manufactured and before being mounted on a circuit board. The plastic packaging can be analogized to plastic shrink-wrap which squeezes the chip, causing stress. The Roberts Patent method involves placing a protective overcoat on the chip or wafer to protect it from the later stress or squeezing forces when the chip is "packaged."

The patent has nine claims, and the disputes in this case center on Claim 9, which is an independent claim and the only asserted claim from the Roberts patent. The following is Claim 9 with the terms in dispute in bold:

In making plastic-encapsulated IC chips formed with an integrated circuit having **stress-sensitive portions,** the **method of reducing stress-induced effects on the performance of the integrated circuit,** comprising:

forming a wafer with a plurality of IC chips including **wire bond pads;**

applying **over the wafer** a **coating of flowable insulating material;**

removing the flowable material from regions of said chips around said bonding pads so as to provide marginal insulation-free regions around each bond pad to laterally separate the wire-bond pads from the insulating material **to assure that wires thereafter bonded to each pad are spaced away and thereby isolated from said insulating material;**

splitting said wafer into separate chips;

bonding wires to the bond pads of said chips; and

encapsulating said coated chips in plastic.

Claim 9, Element 1-"stress-sensitive portions."

Motorola argues that this term should be defined as "portions of the IC circuitry subject to compressive piezo (squeezing) stresses capable of altering unacceptably the electrical performance of the circuits." A.D.I. contends the term means "circuit elements that vary in performance due to applied stresses." Both parties rely upon the summary portion of the patent, including Col. 1: 61-65. Motorola also points to the prosecution history, Amendment B, at pp. 2-3. The primary dispute between the parties appears to be whether the term "stress" is limited to "compressive (piezo) squeezing stresses."

The plain language of the claim does not limit the "stress" to any particular type. That portion of the specification on which Motorola relies (Col. 1: 61-65) does refer to the plastic encapsulation or "packaging" applying piezo (squeezing) stresses capable of altering unacceptably the electrical performance of the circuits. However, that reference does not limit, or re-define, the term "stress," and it would be improper for this Court to import limitations into the claim which are not set out in the claim itself. Elsewhere, the

specification does not limit "stress" to only piezo stresses. Rather, the specification discusses "stresses" in general terms. For example, Col. 1: 66-Col. 2: 9 discusses unlimited "stress variations" which cause certain portions of the circuitry to change their characteristics so as to alter circuit signals beyond desired limits. An example is given of variations in measured offset voltage for certain types of chips. The specification also notes "the present invention is directed to avoiding stress effects on chips packaged in plastic."

The prosecution history upon which Motorola relies does not amount to "clear and unmistakable statements of disavowal" needed to limit the term "stress" to any particular type.

The Court interprets this claim term as follows:

"stress-sensitive portions" means: integrated circuit elements that vary in performance characteristics when subjected to stress.

Claim 9, Element 2-"the method of reducing stress-induced effects on the performance of the integrated circuit

Motorola proposes that this phrase should be defined as "the method of reducing the change in circuit characteristics to stay within close tolerances under stipulated conditions and particularly providing minimal thermal stress affecting these portions of the chip." Motorola relies upon Col. 2: 1-7 of the specification and Amendment B in the file history. However, the referenced portion of the patent, Col. 2: 1-7, simply gives an example of the problem to be solved. Neither the portion of the patent referenced nor the Amendment B indicate that the only stress problems to be addressed by the patent are thermal stresses. The Court interprets this claim term as follows:

"the method of reducing stress-induced effects on the performance of the integrated circuit" means: the method of reducing changes in the characteristics or performance of an IC chip which may result from applied stress.

Claim 9, Element 3-"wire bond pads."

In the Joint Claim Construction Statement, A.D.I. proposed to construe this term as "the area of a metal layer left open for electrical connection to bonds for wires." A.D.I. cited as authority a definition in an undated version of the Sematech Dictionary. A.D.I. also refers to the Roberts patent Col. 2: 10-17 and Col. 4: 52-64,. In a letter dated February 6, 2004, A.D.I. modified its proposed construction to "a metallized area on the surface of a semiconductor device, to which connections can be made." A.D.I. argues that this definition is the same as that offered by Motorola for the term "bonding pad" in the Pelley patent and claims.

Motorola proposes that the term "wire bond pads" means "contact pads to which very fine wires are attached to connect the pads to external leads," citing Col. 1: 39, Col. 2: 10-17, Col. 2: 60, and Fig. 2. As seen from the references to the specification, the Roberts patent uses the term "contact pad" to refer to that structure on the IC chip to which a bonding wire is attached to connect the chip to an external lead. The dispute between the parties now appears to center on whether the "wire bond pad" must involve a *wire* connection.

Figure 2 of the Roberts patent, together with the related descriptions in the specification (see, *e.g.*, Col. 2: 59-60, Col. 3: 54-56), appear to refer to the contact pad 18 as a discrete metal structure, having defined edges, to which wires are connected, as opposed to simply a "metallized area on the surface" of the chip.

Also, at page 90 of the Joint Claim Construction Statement, the parties agree that the phrase "removing the flowable material from regions of said chips around said bonding pads so as to provide marginal insulation-free regions around each bond pad" would mean "removing the flowable insulating material, such as by etching techniques, to provide regions around the **periphery** of each wire bond pad that are free from flowable insulating material." (Emphasis added) This would indicate that the wire bond pad is the patterned metal area to which the contact wires are attached. Otherwise, there could be no "periphery" of the pad free of insulating material. This is consistent with the specification, at Col. 4: 57-62, where it explains that, in one embodiment, "the protective coating is etched out in the regions of the bond pads (including a marginal region around each bond pad ...)."

The Court defines the claim term as follows:

"wire bond pads" means: contact pads to which fine wires are attached to connect the metal layer of which the contact pad is a part to some other point, circuit, or device.

Claim 9, Element 4-"over the wafer."

Motorola would define this term as "covering the entire top of the wafer," while A.D.I. would simply say, "on top of the wafer." Motorola argues that because Claims 1 and 7 do not speak of the insulating material being "over the wafer," but rather only over "the stress-sensitive portions of the chip," there is an implication that Claim 9 should be interpreted to require the flowable insulating material covering the entire top of the wafer. Motorola also refers to Col. 4: 52-58 where the patent describes a procedure of spin coating the protective layer on the wafers, suggesting that such a procedure will result in a covering over the entire top of the wafer. However, the first words of that paragraph are "[I]n another embodiment of the invention." Thus, spin coating is simply one method by which the material may be applied "over the wafer," and it is not proper to import limitations from the specification which are merely descriptions of various embodiments. There is no evidence before the Court that spin coating is the only method by which a wafer may be coated. In fact, claim 10 depends from claim 9 and specifies that the material is applied to the wafer "by spin coating," suggesting that other methods may be used in claim 9 to apply the material.

The plain meaning of the word "over" is "above" or "on top of" and the Court construes this claim term as follows:

"over the wafer" means "on top of the wafer."

Claim 9, Element 4-"a coating of flowable insulating material."

A.D.I. would define this term as "a coating of flowable material that protects the IC chip from stress-induced effects." Motorola would again import a limitation from one of the embodiments in the specification so that the material would be "dispensed onto the entire top of the wafer." The specification indicates embodiments where the coating is applied "over preselected stress-sensitive portions" of the circuit (Col. 2: 18-19); and a coating which is spread around as a very thin layer. Col. 4: 44-46. These two methods are contrasted with the spin coating method. Col. 4: 52-64. As with the phrase "over the wafer," the Court finds no reason to limit this phrase to "the entire top of the wafer." The Court interprets this element of the claim as follows:

"a coating of flowable insulating material" means: a coating of a material which, when applied, flows, or which can be spread, and which, after application, protects the IC chip from stress-induced effects.

Claim 9, Element 5-"to assure that wires thereafter bonded to each pad are spaced away and thereby isolated from said insulating material."

The parties' respective definitions start off in agreement, specifically, that the wires to be bonded will be spaced away from, and isolated from, the flowable insulating material. However, Motorola seeks to add a "result" limitation, namely, "so as to avoid breakage to the contact pads after the chip is encapsulated in plastic." This additional limitation is a statement of a result that might be achieved by the recited structure.

Motorola's reliance upon the description of a particular embodiment and the file history which gives a reason for keeping the insulating material away from the wires if misplaced. It is not proper to import such a limitation into the claim. The Court, therefore, defines this claim term according to its plain meaning, as follows:

"to assure that wires thereafter bonded to each pad are spaced away and thereby isolated from said insulating material" means: to assure that the wires that are later bonded to the bond pad are spaced away from the coating of flowable insulated material.

THE YALLUP PATENT

U.S. Patent No. 5,479,048, the Yallup Patent, is held by A.D.I. and was issued on December 26, 1995. An integrated circuit chip is made on, and supported by, an underlying wafer which is referred to as the "handle wafer." The Yallup Patent teaches a method of dealing with the problem of accumulation of a charge in the handle wafer upon which the integrated circuit has been constructed. The patent also is intended to solve the problem of devices on separate regions of the wafer, such as two transistors, electrically coupling through the handle wafer.

Only the first claim of the four claims of the patent is at issue in this suit. Claim 1, with the disputed terms in bold, is set out below.

An integrated circuit (IC) chip of the type including a **first semiconductive section** with a number of **device regions** laterally disposed throughout the section; **a layer of insulating material underlying said first semiconductive section;** a second semiconductive section **underlying said insulating layer** and serving as a handle wafer to support said insulating layer and said device regions;

Said first semiconductive section being formed with a **plurality of first trenches between at least certain of said device regions** and extending from the chip surface down through said first semiconductive section to said layer of insulating material;

said first semiconductive section being formed with a **plurality of first trenches between at least certain of said device regions** and extending from the chip surface down through said first semiconductive section to said layer of insulating material;

said first trenches being **filled with electrical insulating material which at the bottom of the trench is contiguous to and in contact with said insulating layer** thereby to form electrical insulating material surrounding at least one of said device regions;

and **additional trench** formed in said chip and arranged to extend down through said first semiconductive

section and also through said underlying layer of insulation so that its lower extremity penetrates to the region of said second semiconductive region at a depth beneath the lowest regions of said first trenches;

electrically conductive material filling said additional trench and at **its lower extremity being engaged with and establishing electrical connection to the material of said second semiconductive section serving as said handle wafer;**

metallization means above said additional trench and in contact therewith to **establish electrical connection thereto;** and

means electrically connected to said metallization means to apply a controlling potential through said additional trench to fix the potential of said handle wafer to avoid improper operation of said device regions of the I.C. chip and to prevent accumulation of damaging electrostatic charges in the handle wafer.

Claim 1, Element 1-"first semiconductive section."

A.D.I. proposes to define this term as merely "a semiconductive section." Since this is a disputed term, this restatement of the claim term is not helpful. Motorola proposes "a layer of the IC made of semiconductive material such as silicon." The primary dispute here seems to be A.D.I.'s concern over the use of the word "layer," a disputed term in the Candaleria patent. However, the patents are separate and not related. Reviewing the claim, and the specifications, one skilled in the art would understand that "a first semiconductive section" would be a layer of one or more device regions. The Court will define this term as follows:

"first semiconductive section" means: a layer of the IC chip, made of a semiconductive material, and which may be divided into a number of different regions or areas.

Claim 1, Element 2-"with a number of device regions laterally disposed throughout the section."

Motorola proposes only the ordinary meaning be ascribed to this term, without specifying what it contends the "ordinary meaning" is. A.D.I. points to the specification, in particular, Figure 1F and Column 1: 18-19, Col. 1: 30-34, and Col. 2: 33-42, to argue that a device region should be defined as a region containing electronic components, such as transistors, electrically insulated from other regions that contain electronic components. At the Markman hearing Motorola argued that the term is well understood in the art to mean the regions containing electrical devices, and as such needed no further definition. But, Motorola indicated that if the Court decides to construe the term, Motorola would agree with A.D.I.'s proposed construction to the extent of "a region containing electronic components." This is virtual agreement with A.D.I.'s proposed construction, and the Court will define the term as follows:

"device region" means "a region of the first semiconductive layer or section containing one or more electronic components (such as transistors)" [that is electrically insulated from other regions that contain electronic components].

Claim 1, Element 3-"layer of insulating material underlying said first semiconductive region."

The key term in dispute here is "underlying," which Motorola would define as "immediately beneath and in contact with." Motorola relies upon Col. 1: 19-24 and Figures 1A-1F which show embodiments.

"Underlying" is not a special technical term, even in the context of this patent, and neither party provides any authority for the proposition that "underlying" has a special technical meaning. The ordinary meaning of the word is "lying or situated under." One skilled in the art would understand that chips are generally formed by deposition of layers of various materials on the substrate or wafer. While the chip can be turned in almost any direction, one skilled in the art would understand that as the various layers are applied and the device is constructed, the substrate is considered to be at the "bottom," and succeeding layers are placed "on top."

The plain meaning of underlying does not require "immediately beneath" nor "in contact with." For example, while one layer may immediately "underlie" and be in direct contact with another layer, the handle wafer may underlie any number of layers of metal or semiconductive material. While these various layers may be said to be bonded to the handle wafer, or "supported by" the handle wafer, they are not necessarily in direct contact with it. Motorola has not pointed to any evidence in the specification or the prosecution history suggesting that the patentee intended a special meaning for the term.

The Court interprets this term of the claim as follows:

"layer of insulating material **underlying** said first semiconductive section" means: a layer of material that generally does not conduct electricity which is situated, or positioned, under the first semiconductive section or layer, with or without intervening layers.

Claim 1, Element 4-"a second semiconductive section underlying said insulating layer."

The words immediately following this phrase are "serving as a handle wafer to support said insulating layer and said device regions." The parties agree that the handle wafer is "a supporting bottom region of a silicon-oninsulator wafer which supports the insulating layer and the device regions." As discussed above, it is by convention that the handle wafer is at the "bottom" and the other layers are "above." Accordingly, for the reasons expressed above, the Court will interpret this claim term as follows:

"a second semiconductive section **underlying said insulating layer"** means: a layer of the IC chip made of a semiconductive material, which is under the insulating layer, with or without intervening layers.

Claim 1, Element 5-"a plurality of first trenches between at least certain of said device regions."

Both parties agree that "trench" is defined in the Sematech Dictionary as "a deeply etched area used to isolate one area from another or to form a storage capacitor on a silicon wafer." Motorola proposes that the rest of the term be construed to be "a plurality of trenches, each of which separates one device region from the adjacent device region." There is nothing in the claim, nor in the specification, that indicates that the definition in question should be limited to trenches that separate a device region from an "adjacent" device region. The claim language simply requires trenches "between at least certain of said device regions," which does not necessarily require that every region is isolated from its immediately adjacent neighbor. A trench may separate one device region from another device region which is immediately adjacent to it, or it may separate the device region only from a device region which is further removed. The Court interprets this claim element as follows:

"a plurality of first trenches between at least certain of said device regions" means: two or more deeply etched areas used to separate some of the device regions from other device regions.

Claim 1, Element 6-"contiguous to and in contact with."

Claim 1 recites that the first trenches are filled with electrical insulating material which at the bottom of the trench is "contiguous to and in contact with" the insulating layer. Motorola utilizes Webster's Ninth New Collegiate Dictionary to argue that the term "contiguous" should be defined as "touching or connected throughout in an unbroken sequence." A.D.I. cites the American Heritage College Dictionary, which defines the term as "sharing an edge or boundary; touching." The Merriam-Webster Dictionary defines "contiguous" as "being in actual contact: touching along a boundary or at a point." The Court notes that both of the proposed constructions, as well as the definition from the Merriam-Webster Dictionary, use as an alternative "touching." Nothing in the specification or file history suggests the term should have any meaning other than its ordinary meaning. In light of the language of the claim, and the description set out in the specification and in the diagrams, the Court will define this claim term as follows:

"**contiguous** to and in contact with" means: next to, and in contact with.

Claim 1, Element 7-"filled with electrical insulating material which at the bottom of the trench is contiguous to and in contact with said insulating layer."

The dispute here is whether Motorola's proposed construction, which states that the electrical insulating material "completely fills" the trench, including the bottom of the trench, is correct. Motorola cites only to Fig. 1E of the patent. A.D.I. argues that "[t]here is nothing in the ordinary meaning of the term 'filled' that requires an absolute condition, such as being 'completely' filled," reciting an example of a glass being "filled" with water without being "completely filled." Webster's New College Dictionary (1995) defines "fill" as "1. to put into as much as can be held (*fill a heater*) (*fill a sack with grain*). 2.a. to plug up (*e.g.,* an opening). B. to repair a cavity of (a tooth)." There is evidence that, when trenches are "filled," the fill materials often do not completely fill the trench, and that unintended voids may exist in the material. Hence, in the context of the Yallup patent, the word "fill" would not be understood to require a perfect, absolute condition. Rather, the word, in this context, indicates a condition of "substantially full."

The Court will interpret this claim term as follows:

"filled with electrical insulating material which at the bottom of the trench is contiguous to and in contact with said insulating layer" means: the first trenches are filled with an electrical insulating material which touches the insulating layer at the bottom.

Claim 1, Element 8-"additional trench."

The plain meaning of "additional" is "another." As discussed above, the parties agree the word "trench" is defined in the Sematech Dictionary as "a deeply etched area used to isolate one area from another or to form a storage capacitor on a silicon wafer." The patent specification, insofar as it describes the "first trenches," uses the word "trench" consistent with the Sematech definition. For example, in Figs. 1A-1F and at Col. 2:33-48, trenches 10 are filled with insulating material, and they "establish the required isolation barriers between the device regions 18." However, the specification also describes a "trench" 10A (see, *e.g.,* Fig. 1D) that does not necessarily isolate device regions, but does provide a means for establishing electrical connectivity between the handle wafer 22 and the top side of the chip. See Col. 2:62-3:4, Col. 3:15-18 and Col. 3:21-24. Hence, Motorola argues that the term "additional trench" necessarily implies a trench different from the first trenches, and refers to various figures in the patent. However, it is not proper to import limitations from the specifications into the claim based simply on disclosed embodiments. Therefore, the

Court will interpret this term according to its plain meaning, as follows:

"additional trench: means "another deeply etched area."

Claim 1, Element 9-"its lower extremity penetrates to the region of said second semiconductive region at a depth beneath the lowest regions of said first trenches."

Citing the prosecution history, Motorola interprets this phrase as requiring the bottom of the "additional trench" to be "below the bottom" of the insulating layer. However, the language of the claim itself requires only that the bottom of the "additional trench" is in contact with the handle wafer (the second semiconductive region) so that an electrical connection can be formed. The description in the specification is consistent with the claim language. And the argument from the prosecution history on which Motorola relies does not indicate a clear disavowal of the plain meaning of the claim language. Accordingly, the Court will interpret this claim term as follows:

"its lower extremity penetrates to the region of said second semiconductive region at a depth beneath the lowest regions of said first trenches" means: the bottom of the additional trench extends below the lowest reaches of the first trenches, and it extends to the handle wafer so that contact may be made with the handle wafer.

Claim 1, Element 10-"electrically conductive material filling said additional trench."

There are two principal disputes with respect to this claim phrase. First, Motorola argues that the word "filling" means "completely filling," as before. A.D.I. contends that "filling" does not require "completely filling." Second, Motorola argues that the conductive material must be in contact with both the first and second semiconductive sections, whereas A.D.I. contends that the claim does not require the conductive material to be in contact with the first semiconductive section.

As before, the ordinary dictionary meaning of the word "filling" is "putting into (or having) as much as can be held." However, as with the word "filled" discussed above, in the context of the Yallup patent, one of ordinary skill in the art would understand that the word "filling" would not require a perfect, absolute condition. Thus, the plain meaning of the phrase in the context of the Yallup patent would be "being substantially filled with electrically conductive material." The description in the specification is consistent with this plain meaning, and the prosecution history contains no clear disavowal of the plain meaning. Moreover, the phrase does not suggest or require that the electrically conductive material is in contact with the first semiconductive section, nor does the disclosure in the specification mandate adding such a limitation to the claim.

The court interprets this term as follows:

"electrically conductive material filling said additional trench" means: material through which an electric charge or current can easily flow substantially fills the trench to provide a path for current from the handle wafer to the metal at the top.

Claim 1, Element 11-"at its lower extremity being engaged with and establishing electrical connection to the material of said second semiconductive section serving as said handle wafer."

The parties claim that this term is disputed; but based upon their definitions, the Court cannot determine

why. Neither of the parties addressed this phrase in their briefing. Both definitions capture the apparent intent of the claim, namely, that the lower extremity of the electrically conductive material is in electrical contact with the handle wafer. This is consistent with the Court's construction of "filling the additional trench" set out above. The Court interprets this claim term as follows:

"at its lower extremity being engaged with and establishing electrical connection to the material of said second semiconductive section serving as said handle wafer" means: the electrically conductive material, at its lower extremity, touches and makes electrical contact with the handle wafer.

Claim 1, Element 12-"metallization means ... to establish electrical connection thereto."

The parties agree that this is a means-plus-function element. Therefore, under 35 U.S.C., Section 112, Paragraph 6, the "metallization means" covers the embodiments set out in the specification and equivalents thereof. The recited function is to establish electrical connection to the additional trench. Additional recitation requires that the "metallization means" be "above said additional trench and in contact therewith," that is, in contact with the additional trench.

Every embodiment shown in the patent shows the metal of the "metallization means" not only in direct contact with the electrically conducting material in the trench, but also in indirect contact with the electrically conductive material by way of the shoulders of the trench. In Figure 1 F, the metal 44 is in electrical contact with the polysilicon ("POLY") in the trench 10A. Col. 3:15-18. The metal 44 is also in electrical contact with the horizontal shoulder regions 46 of the device regions 18. Col. 3:18-21. These device regions 18 are, in turn, in contact with the polysilicon ("POLY"). Col. 3:58-64. See also Col. 2:55-61.. In Figure 3, another embodiment, the metal 44 is in electrical contact with the shoulders 66 of the device regions 68, and contact implants 62 have been placed in the shoulder regions to enhance the conductivity between the metal 44 and the "POLY" in the trench 10A. Col. 3:39-48. As stated at Col. 3: 42-45, electrical connection to the shoulder regions can be established through contact between the metallization and the horizontal side surfaces of the adjacent device regions. With this arrangement the two adjacent device regions will be dedicated to the function of making contact with the handle wafer.

A.D.I. argues that the contact of the metal with the shoulders of the trench should be ignored. However, the specification is very clear that, in both embodiments (Fig. 1F and Fig. 3), the function of establishing electrical connection to the additional trench is by way of direct contact between the metal and the POLY, as well as by way of indirect contact through the shoulder regions of the additional trench.

Accordingly, the Court finds that the structure in the specification that performs the function recited for the **"metallization means"** is, as shown in Fig. 1F and Fig. 3, a metal layer in contact with the electrically conducting material in the additional trench, and in contact with the shoulders of the trench, to establish an electrical connection to that conducting material and thus to the handle wafer. The "metallization means" is construed as covering that structure and equivalent structures.

Claim 1, Element 13-"means electrically connected to said metallization means to apply a controlling potential through said additional trench to fix the potential of said handle wafer."

The parties agree that this is a means-plus-function element, with the recited function being for "apply[ing] a controlling potential through said additional trench to fix the potential of said handle wafer." The parties agree that the described structure includes a bond pad. A.D.I. argues the "means" also includes "electrical interconnects to electrically connect the bond pad to the 'metallization means.' " A.D.I. cites Col. 3:21-31

and Figure 2. Motorola argues the "means" includes, in addition to the bond pad, "associated wiring connecting the metallization means, and the device region, to a pin of the chip package, which is connected to a positive power supply voltage." Motorola cites Col. 3:21-31 and Col. 4:40-42.

The claim is directed to a chip. The structure on the chip that performs the function recited in the claim includes the bond pad and the electrical connections between the bond pad and the "metallization means." Including wiring external to the chip and the power supply in this means-plus-function analysis results in including components that are beyond the chip itself. Accordingly, the Court interprets this element of the claim as follows:

"means electrically connected to said metallization means to apply a controlling potential through said additional trench to fix the potential of said handle wafer" means: a bond pad and electrical connections between the bond pad and the "metallization means."

Claim 1, Element 14-"to avoid improper operation of said device regions."

The word "avoid" means to shun or to keep from happening, *i.e .,* to prevent or reduce the likelihood of," the word "improper" means "irregular or abnormal," and "operation" means "an act, process or way of operating; the condition of being operative or functioning; a process or series of acts aimed at producing a desired result or effort." Webster's II New College Dictionary 1995. Thus, the plain meaning of this phrase is to prevent or reduce the likelihood of irregular or abnormal functioning of the device regions, or components in the device regions.

Both parties cite to the specification, at Col. 1: 30-34, which discusses "one feature of die lectric isolation," that being electrical coupling in such a way that the operation of devices in the device regions can be modified. However, the plain meaning of the claim language is broader than this "one feature." Thus, the plain meaning would not be limited, as Motorola's definition would do, to eliminate electrical coupling between device regions or the handle wafer. Moreover, the argument from the prosecution history does not amount to a clear disavowal of the plain meaning of the phrase. Specifically, A.D.I. distinguished application claim 11 (issued claim 1) from the art of record by arguing that the references did not show any means to control the potential of the handle wafer. A.D.I. argued that the pending claim recites structure that was not disclosed in or suggested by the cited references. A.D.I.'s statement that the recited structure "prevents or reduces intercoupling between device regions and prevents damage from charge accumulation in the handle wafer" does not represent a clear disavowal of the ordinary meaning of the phrase "to avoid improper operation of said device region."

The Court construes this claim term as follows:

"to avoid improper operation of said device regions" means: to prevent or reduce the possibility of irregular or abnormal operation of one or more devices in the device region.

Claim 1, Element 15-"to prevent accumulation of damaging electrostatic charges in the handle wafer."

Both parties agree at the beginning of their proposed definitions that this phrase involves avoiding accumulation of electrostatic charges in the handle wafer. Motorola would add that this accumulated charge "causes damage to the materials because of absence of current path to ground." While this may be one of many reasons why damage may occur, it does not set out a description of the device. A.D.I. adds that the

accumulated charge "could decrease the level of performance or reliability of the device regions." The specification, at Col. 1: 34-37, indicates that accumulation of a charge in the handle wafer could lead to electrostatic damage of one or more regions. The Court interprets this claim element as follows:

"to prevent accumulation of damaging electrostatic charges in the handle wafer" means: To prevent accumulation of an electrostatic charge in the handle wafer that could lead to damage to one or more isolation regions.

THE PELLEY PATENT

U.S. Patent Number 5,040,144, the Pelley Patent, is held by Motorola and was issued on August 13, 1991. It teaches a method of improving distribution of power to the various blocks of an integrated circuit by adding certain power distribution lines. Simplistically, this can be conceptualized by imagining a power source at the top of a page with a power line running horizontally along the top of the page. Power lines then run vertically from the top power line to the various blocks located on the page. The blocks at the bottom of the page are further from the power source than the blocks at the top of the page, resulting in a difference in power delivered to the various blocks. Generally speaking, the patent attempts to solve this problem by adding a series of intersecting power lines that run horizontally across the page forming a grid. The chip does not have to be any larger to accommodate the additional power lines because the horizontal grid lines are in a different layer than the first set of power supply lines, and the additional lines occupy otherwise unused space.

Disputed Claim Terms of the Pelley Patent

The parties dispute terms in claims 1, 3, 4, 5, and 6. Claims 1, 3, and 4 are set out below with the disputed terms printed in bold.

Claim 1-A **memory** having **a plurality of subarrays** aligned in a first direction, comprising a plurality of **metal decoding lines** crossing the plurality of subarrays in the first direction, said plurality of metal decoding lines formed in a **first predetermined layer;**

a plurality of metal **power supply lines** crossing said plurality of subarrays in a second direction, said second direction **substantially orthologna**l to said first direction, said plurality of metal power supply lines formed in a **second predetmined layer** different from said first predetermined layer; and

a plurality of metal **grid lines** between said metal decoding lines and intersecting and coupled to said metal power supply lines, said plurality of metal grid lines formed in said first predetermined layer.

[These terms are agreed in the Joint Claim Construction Statement.]

Claim 3-The memory of Claim 1 wherein said metal power supply lines and said metal grid lines provide a **power supply voltage terminal** to the memory.

Claim 4-An integrated circuit memory with [*See* Certificate of Correction] a plurality of **memory blocks,** each memory block comprising a plurality of **memory cells,** comprising:

A **bonding pad,** for providing an interconnection point to a power supply voltage terminal, said **power supply voltage terminal** external to the integrated circuit.

Claim 1, Element 1-"A memory having a plurality of subarrays aligned in a first direction."

For the term "memory," Motorola proposes the definition in the *I.E.E.E. Standard Dictionary of Electrical and Electronic Terms* (4th Ed.) (1988): "Any device in which information can be stored, sometimes called a memory device." Since the patent itself does not state a definition for "memory" and neither the specification nor the prosecution history indicates an unusual meaning for the term, a contemporaneous technical dictionary is a useful guide. See Texas Digital Sys., Inc. v. Telegenix, Inc., 308 F.3d 1193, 1202 (Fed.Cir.2002).

A.D.I. argues that "memory" necessarily implies "random-access memory," which is one particular type of "memory." As authority, A.D.I. relies on two 1995 dictionary references. First, these dictionaries are dated four years after the patent issued. Additionally, "random-access memory" is given as an example or type of memory, but not as the definition of "memory" generally.

A.D.I. argues that, in the case of the Garde patent, another patent-in-suit, the parties have agreed to a definition for "memory" that is the same as A.D.I. proposes here. But the Garde patent and the Pelley patent are unrelated to one another. Moreover, the application leading to the Garde patent was filed over six (6) years after the Pelley patent application, and the Garde patent issued almost eight (8) years after the Pelley patent issued.

At the hearing, A.D.I. pointed out that, in a Certificate of Correction, Motorola intentionally changed the preamble of claim 4 from "an integrated circuit" to "an integrated circuit *memory,*" indicating Motorola appreciated the difference between an integrated circuit *with* memory and an integrated circuit memory. A.D.I. argues Motorola now asserts there is no difference, even though the change in the preamble is consistent with the ordinary meaning of the word. The change noted in the Certificate of Correction applies to claim 4. The preamble of claim 1 was unchanged, and it refers simply to a "memory." Hence, the change brought about in the Certificate of Correction does not alter the plain meaning of the term "memory."

Regarding the phrase "plurality of subarrays," the parties agree that "a plurality of" means two or more. A.D.I. argues that the word "subarray" is indefinite because it "does not have a plain meaning to those of ordinary skill in the art" and "the patent fails to point out, with any particularity, the scope or meaning of that term." Alternatively, A.D.I. argues that if "subarrays" is not indefinite, it means simply "a group of elements forming a complete unit," a definition taken from Merriam-Webster.

Motorola contends that "subarrays" should be defined as "subordinate parts of an array," and Motorola would define "array" to mean "an arrangement of many memory cells defined by physical and/or logical boundaries." For support, Motorola cites to the specification, Col. 2:42-60, and Figure 1. There, the specification describes, and Figure 1 shows, four "arrays," each comprising a group of memory cells, and each of which is further divided into smaller groupings of memory cells. Each of the smaller groupings is referred to as a "memory block."

A.D.I.'s own definition of "array" is "a group of elements forming a complete unit" "This comports with standard English usage as well as the use of the term in the specification. In standard English usage the prefix "sub" means subordinate.

The Court will interpret this disputed claim term as follows:

"a **memory** having **a plurality of subarrays** aligned in a first direction" means: A device in which information can be stored which has an array, or a grouping, of memory cells, the array being subdivided into two or more smaller groupings of memory cells.

Claim 1, Element 2-"first predetermined layer."

This term was disputed, but at the Markman hearing the parties agreed that this term should be defined as follows:

"first predetermined layer" means a metal layer, whose design is determined beforehand.

Claim 1, Element 3-"power supply lines" as distinguished from "grid lines." "

The claim describes a grid of intersecting power conducting lines. Those oriented in one direction are referred to as "power supply lines," while those oriented in another direction are referred to as "grid lines."

Motorola proposes that "power supply lines" are "lines that supply power (*e.g.,* VSS or VDD) to the subarrays," and that "grid lines" are "lines that, in combination with the metal power supply lines, form a grid for providing power to the memory." Motorola also argues the grid formed by the power supply lines and grid lines "approximates a metal plate that decreases resistance between a given point within a subarray and the bonding pad." Motorola relies on several passages from the specification.

A.D.I. contends that the "power supply lines" are those lines with "direct connections to circuit elements (*e.g.,* memory cells)." A.D.I. proposes that the "grid lines" would also be power supply lines but would not be directly connected to circuit elements, such as the memory cells. A.D.I. bases its argument, in part, upon the specification, particularly Col. 9: 25-27. This description is directed to one particular embodiment, and it indicates that the power supply lines are coupled to the underlying memory cells so that the grid lines do not themselves provide power to the memory cells.

The claim language simply indicates that there are two sets of lines, one of which is called "power supply lines" and one of which is called "grid lines." Additionally, there is a third set of lines called "metal decoding lines." Two of these sets of lines are in the same layer of the device, and the third is in a separate layer, but connected to lines in the first layer. Nowhere in the claim is there an indication that only the "metal power supply lines" are connected to the memory cells, and it would be improper to import such a limitation into the claims from the specification. Claim 1 does indicate that the metal grid lines are "intersecting and coupled to said metal power supply lines," but claim 1 does not specify whether the power supply lines or the grid lines are connected to memory cells, nor does it specify that one set or the other is connected to memory cells. Moreover, the specification indicates that while "in a preferred embodiment" the grid line (123) is located in a "second metal layer," while the power supply line (114) is located in a "first metal layer." However, "the order of the layers could be reversed." Col. 9: 28-30.

The Court will interpret these disputed claim terms as follows:

"Power supply lines" and **"grid lines"** mean: Two different sets of lines through which electric power can be provided, running perpendicular to each other to form a grid which supplies power to the elements of the array or subarray in the device.

Claim 2, Element 1-"global word lines."

Originally the parties disagreed, with A.D.I. proposing to limit the construction to "a divided word line" architecture. However, at the Markman Hearing the parties agreed as follows:

"global word lines" means: word lines that are input to the word line decoder of a memory block.

Claim 2, Element 2-"local word lines."

The parties are now agreed on this term as follows:

"local word lines" means word lines that are output of the word line decoder of a memory block.

Claims 3, 4, & 6, Element 1-"Power supply voltage terminal."

This claim term is used in Claims 3, 4, and 6. However, in Claim 4 the phrase is "said power supply voltage terminal **external** to the integrated circuit." (Emphasis added). Since Claim 6 is dependent upon Claim 4, it necessarily incorporates the concept that the terminal is "external." On the other hand, Claim 3 does not limit itself to a terminal which is external to the integrated circuit.

The parties are agreed that a power supply voltage terminal is a point or terminal at which power is supplied. The Court interprets this disputed claim term as follows:

"Power supply voltage terminal" means in Claim 3 a point or terminal at which power is supplied. In Claims 4 and 6 this term means a point or terminal external to the integrated circuit at which power is supplied.

Claims 4, 5 & 6, Element 1-"integrated circuit memory."

A.D.I. proposes to define this term as "a memory chip," relying upon the *McGraw-Hill Dictionary of Scientific and Technical Terms* (5th Ed.1994). The Court notes that this reference is dated three years after the date the patent issued. Motorola proposes a definition from the *I.E.E.E. Standard Dictionary of Electrical and Electronic Terms* (4th Ed.1988), specifically, "a memory within an integrated circuit." There is no indication in the specification or in the prosecution history that the word is used in anything other than its ordinary meaning. The Court will define this claim term as follows:

"Integrated circuit memory" means: a memory within an integrated circuit.

Claims 4, 5 & 6, Element 2-"memory blocks."

Motorola proposes to define this term as "a set of memory cells with a common set of local word lines." A.D.I. proposes "a number of memory cells and their read/write circuitry." Both parties rely upon Col. 2: 54-60 and Figure 1 of the patent. Figure 1 is described as "a memory." Col. 2: 42. "Memory blocks" grouped in arrays are described as being part of the "memory." Col. 2: 42-60. There is nothing to indicate that a memory block is anything other than a set of memory cells.

The parties agree at page 33 of the joint claim construction statement that a "memory cell" means "a single storage element of a memory together with associated circuits for storing and reading out one bit of

information." Therefore, the Court defines this disputed term as follows:

"memory block" means a group of memory cells which are associated or connected in a unit, a plurality of memory blocks being grouped to form a memory.

Claim 4, Element 2-"bonding pad."

A.D.I. proposes the definition to be "the area of a metal layer left open for electrical connection to bonds for wires." A.D.I. cites a *Sematech Dictionary,* but does not give a date for the edition referred to. Additionally, the definition quoted from that dictionary is different from A.D.I.'s proposed construction. The *Sematech Dictionary* definition is "relatively large metal areas on a die used for electrical contact with a package or probe pins."

Motorola relies upon the *McGraw-Hill Dictionary of Scientific and Technical Terms* (4th Ed.1989) which defines a "bonding pad" as: "a metallized area on the surface of a semiconductor device, to which connections can be made." This dictionary is dated the same year that the Pelley patent application was filed.

There is no indication in the specification or the prosecution history that a definition other than ordinary usage should be assigned to "bonding pad." The Court will define this disputed term as follows:

"bonding pad" means: a metallized area on the surface of a semiconductor device to which connections can be made.

CONCLUSION

The jury should be instructed in accordance with the court's interpretation of the disputed claim terms in the Goldman, Candelaria, Roberts, Yallup, and Pelly patents.

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