United States District Court,
N.D. California, San Jose Division.

IKOS SYSTEMS, INC. and Massachusetts Institute of Technology,
Plaintiffs.
v.
AXIS SYSTEMS, INC,
Defendant.

No. C 01-21079 JW

June 18, 2002.

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ORDER RE CLAIM CONSTRUCTION

[Docket No. 32]

JAMES WARE**, District Judge.**

Plaintiffs Ikos Systems, Inc. ("Ikos") and Massachusetts Institute of Technology ("MIT") initiated this patent infringement suit against Defendant Axis Systems, Inc. ("Axis"). Plaintiff filed a complaint on February 7, 2001, asserting infringement of three United States Patents: U.S. Patent No. 5,596,742 (the "'742 Patent") and U.S. Patent No. 5,761,484 (the "'484 Patent"), both entitled "Virtual Interconnections for Reconfigurable Logic Systems"; and U.S. Patent No. 5,649,176 (the "'176 Patent"), entitled "Transition Analysis and Circuit Resynthesis Method and Device for Digital Circuit Modeling." The technology at issue relates to the field of electronic design automation. The parties participated in a Markman hearing before this Court on May 3, 2002.

Claim construction is purely a matter of law, to be decided exclusively by the Court. Markman v. Westview Instruments, Inc., 517 U.S. 370, 387 (1996). Claims are construed from the perspective of a person of ordinary skill in the art at the time of the invention. Markman v. Westview Instruments, Inc., 52 F.3d 967, 986 (Fed.Cir.1995). To determine the meaning of the claim terms, the Court initially must look to intrinsic evidence, that is, the claims, the specification, and, if in evidence, the prosecution history. Autogiro v. United States, 384 F.2d 391 (Ct.Cl.1967). The Court must look first to the words of the claims themselves. *See* Vitronics Corp. v. Conceptronic, Inc., 90 F.3d 1576, 1582 (Fed.Cir.1996). These words are to be given their ordinary and customary meaning unless it is clear from the specification and prosecution history that the inventor used the term with a different meaning. *Id*. The claims should be interpreted consistently with the specification. *See* Renishaw PLC v. Marposs Societa' Per Azioni, 158 F.3d 1243, 1250 (Fed.Cir.1998).

Arguments and amendments made during prosecution of a patent application limit claim terms so as to exclude any interpretation that was disclaimed during prosecution. Southwall Tech., Inc. v. Cardinal IG Co., 54 F.3d 1570, 1576 (Fed.Cir.1995).

Where intrinsic evidence alone resolves any ambiguity in a disputed claim term, it is improper to rely on extrinsic evidence. Vitronics, 90 F.3d at 1583, 1585. However, extrinsic evidence may be considered in the rare instances where the intrinsic evidence is insufficient to enable the court to construe disputed claim terms. Id. at 1585.

A. The '742 and '484 Patents

1. "Virtual Interconnections", "Static", "Statically Routed Communication Network", "Pipelined", "Multiplexed", "Time-Multiplexed", "Phase"

A major point of contention with respect to the '742 and the '484 Patents centers on the definition of "virtual interconnection(s)," a term found in each of the independent claims of the '742 Patent (Claims 1, 27, 32, and 34) and most of the independent claims of the '484 Patent (Claims 1, 21, 23, and 28) currently being asserted by Plaintiffs. Plaintiffs and Defendant agree that this term was coined by the inventors and has no clear meaning to those of ordinary skill in the art. The parties hence look to the specifications and prosecution history of the patents for their definitions.

Plaintiffs Ikos and MIT construe a "virtual interconnection" as "a logical electrical connection implemented by sharing an inter-module connection with other logical electrical connections." Defendant Axis argues that Plaintiffs' definition is unduly broad and would encompass any multiplexing of signals between logic modules, including the prior art. Defendant looks to the preferred embodiments of the '742 Patent and construes "virtual interconnections" to mean "logical connections that result from the application of the technique of statically communicating synchronous logical signals between logic modules through a single pin in a multiplexed, pipelined fashion wherein each logical signal is scheduled for a specific cycle of the pipeline clock." While the Court believes that Plaintiffs' definition is unduly broad, Defendant's construction appears largely in keeping with the language of the patents. The specification of the '742 Patent relied upon by Plaintiffs for their construction indicates that "virtual interconnections overcome pin limitations by intelligently multiplexing each physical wire among multiple logical wires and pipelining these connections at the maximum clocking frequency of the FPGA." ('742 Patent at 2:9-14.) Substituting Plaintiff's definition in place of "virtual interconnections" would cause this and similar phrases throughout the patents to lose their meaning. The Court finds that the intrinsic evidence supports Defendant's proposition that virtual interconnections are established "via a pipelined, statically routed communication network." ('742 Patent at 4:52-59; '484 Patent at 5:7-14.) Moreover, the specifications state unequivocally that "the use of virtual interconnections is limited to synchronous logic." ('742 Patent at 5:36-37; '484 Patent at 5:62-63.) The Court construes a "**virtual interconnection**" as "a logical connection resulting from the application of a technique that creates multiple logical connections between logic modules through a single pin by sending time-multiplexed, pipelined, synchronous logical signals over a statically routed communication network." FN1

FN1. The Court understands "logical signals" to be signals that originate from the performance of a logic function, such as an "AND gate" or "OR gate".

The Court defines "**static**" to mean "that all data movement is determined and optimized at compile-time." ('742 Patent at 1:45-47; '484 Patent at 1:44-46.) The Court construes "**statically routed communication**

network" consistent with the definition of "static" to mean that "communication pathways, including the transmission of signals across the pins, are established at compile-time based on an analysis of the signals in the circuit design before the FPGAs are configured."

The Court construes "**pipelining**" to mean "transmitting different logical signals sequentially in a signal stream wherein each logical signal is transmitted in the same phase." The Court's construction of "pipelined" is consistent with the intrinsic evidence and combines elements of both the Plaintiffs' and Defendant's definitions. ('742 Patent at 4:50-52; '484 Patent at 5:5-7.) "**Pipelined**" means "transmitted through the technique of pipelining."

The Court construes "**multiplexing**" consistent with its well-understood usage to mean "the sharing of a physical wire or pin among multiple logical wires." In the context of virtual interconnections, the term "multiplexing" is generally used to refer to the concept of time-multiplexing. ('742 Patent at 2:9-12, 4:50-52, 5:31-33; '484 Patent at 2:21-24, 5:5-7, 5:58-61.) Although the term "time-multiplexed" is not specifically defined in the '742 and the ' 484 Patents and is mentioned only in the claims, the specifications provide an effective construction of the term in their discussion of multiplexing and virtual interconnections. ('742 Patent at 2:9-12, 4:50-52, 5:31-33; '484 Patent at 2:21-24, 5:5-7, 5:58-61.) The Court construes "**time-multiplexing**" to signify "a form of multiplexing in which time is used to control the transmission of different logical signals through a pin wherein each logical signal is communicated across a different phase." The term "**multiplexed**" means "transmitted through the technique of multiplexing." The Court adopts Defendant's definition of a "**multiplexer**" as a "device that generates multiplexed signals."

The Court adopts Plaintiffs' definition of "**phase**" as "a period within a target clock period during which logic evaluation and communication between modules are performed."

2. "***Static Virtual Interconnections***"

Plaintiffs argue that the existence of the term "static virtual interconnections" in some claims of the '484 Patent negates Defendant's argument that virtual interconnections are inherently static. ('742 Patent at 5:20; '484 Patent at 5:46.) Plaintiffs argue that the inventors "purposefully added the term 'static' to describe virtual interconnection when they intended to limit the invention to having a static or fixed nature." (Pl. Reply Brief, at 7.) The Court finds several problems, however, with Plaintiffs' reasoning. First, Plaintiffs acknowledge that they are not construing the term "static" in the same manner as Defendant, namely to refer to the determination of data movement at the time of compilation. Instead, Plaintiffs argue that "static" refers to "the *route* a logic signal takes or the *location* of a virtual interconnection not changing." (Pl. Reply Brief, at 8.) In this context, a signal propagated through a "static virtual interconnection" will always travel via the same predetermined path. While Plaintiffs' construction may differentiate "static virtual interconnections" from "virtual interconnections," Plaintiffs' definition of "static" is distinct from the definition proffered by the Defendant and therefore does not necessarily nullify Defendant's definition of "virtual interconnection". Second, the Court construes "static" to refer "to the fact that all data movement can be determined and optimized at compile-time," consistent with the definition given in the specifications. ('742 Patent at 1:45-47; '484 Patent at 1:44-46.) In order to avoid the unsupported assignment of two separate definitions to the same term within the same patents, the Court must reject Plaintiffs' construction. Finally, the prosecution history of the patents in question lead the Court to conclude that the existence of the term "static virtual interconnections" in some claims of the '484 Patent does not negate, but rather reaffirms and emphasizes, the inherently static nature of "virtual interconnections". (Def. Brief, at 14.) The term "**static virtual interconnections**" is construed to have the same meaning as "virtual interconnections" by

the Court.

3. "Communication", "Communication Path"

Plaintiffs construe "**communication**" as "the transmission of information from one point to another." The Court adopts Plaintiffs' definition and rejects Defendant's suggestion that the modifier "meaningful" be added before the word "transmission".

The parties agree on, and the Court adopts, the definition of "**communication path**" as "a route over which signals are communicated."

4. "Statically Communicating"

The term "statically communicating" only appears in Claim 17 of the '484 Patent, the only independent claim in either the '484 Patent or the '742 Patent that does not recite "virtual interconnections." The Court construes "**statically communicating**" to mean "communicating in a manner in which all data movement is determined and optimized at compile-time and the communication patterns repeat in a predictable fashion." This construction is based on the specifications in the patents that address the term "static" and its meaning in the context of communications. ('742 Patent at 1:44-46, 5:19-21; '484 Patent at 1:43-45, 5:45-47.)

5. "Configurer"

Plaintiffs construe "configurer" to mean "a system including software that implements a compiler to realize logic circuit elements in a reprogrammable logic module." Defendant defines the term as "a system or element that configures the logic system to perform a desired logic operation or calculation." The Court adopts a modified form of the Defendant's construction of "**configurer**" to mean "a system that configures the logic system to perform a desired logic operation or calculation."

6. "Intermodule Dependencies", "Interpartition Dependencies"

Plaintiffs construe "**intermodule dependencies**" and "**interpartition dependencies**" to refer to "a relationship between two signals in different logic modules/partitions whereby the value of one signal in one logic module/partition depends on the value of the other signal in the other logic module/partition." Defendants essentially argue that the phrase "of a synchronous logic design" should be added to qualify the term "modules/partitions" to limit the above definition. The Court adopts Plaintiffs' definition without the qualifying language proposed by Defendant.

7. "System Clock Period" (also called "Pipeline Clock Period")

Plaintiffs construe "system clock period" as "the period of the clock signal providing a high frequency of operation in a logic module within the reconfigurable electronic system." Defendant construes the term to mean "the period of a fixed frequency clock signal that controls the pipelining of signals within a phase of the target clock (i.e., the period of the pipeline clock)." The Court adopts a modified form of Defendant's definition of "**system clock period**" to mean "the period of a clock signal that dictates the maximum rate at which signals in the electronic system change value and controls the pipelining of signals within a phase of the target clock (i.e., the period of the pipeline clock)." ('742 Patent, Claims 7-9, at 6:7-9; '484 Patent, Claim 6.)

B. Claims of the '176 Patent

1. "Environment", "Environmental"

Plaintiffs construe "environment" to mean "a circuit or system external to the configurable logic system with which the configurable logic system interacts (e.g., a host workstation or a target system)." Defendant contests the inclusion of the "host workstation" in the definition of environment and argues that the claims and specifications of the '176 Patent restrict the definition of environment to a circuit or system "in which the circuit design implemented in the configurable logic is intended to operate (i.e., a target system)." The Court agrees with Plaintiffs that the term environment is used in the specifications to refer both to a target system, i.e., "the intended environment" or "the environment in which the logic system is intended to ultimately function," and a host workstation, depending upon the context. ('176 Patent at 1:41-50, 10:65-66.) For example, in discussing verification systems such as "hardware accelerators," the specifications refer to a host workstation that is modeling the target system in software as the "environment." ('176 Patent at 1:41-50.) In such target-less emulation, the host workstation assumes the role of the "intended environment" referred to in the specifications. *Id*.

Defendant highlights a potential problem with the inclusion of "host workstation" in "environment" even under limited circumstances. The specifications require the internal clock, which forms a part of the configurable logic system, to be "invisible to the environment." ('176 Patent at 3:12-13.) This condition would preclude the host workstation, which is necessarily aware of the internal clock as it configures the configurable logic system, from being a part of the environment. The Court agrees with Plaintiffs, however, that in the context of hardware accelerators and target-less emulation, the part of the host workstation simulating the target can still be construed as the "environment" and considered separate from the part configuring the configurable logic system.

The Court construes "**environment**" to mean "a system or circuit external to the configurable logic system, and external to the host workstation where a separate target system is present, in which the circuit design implemented in the configurable logic is intended to operate."

2. "Environmental Timing Signal"

Plaintiffs would like the Court to construe an "environmental timing signal" as "a timing signal from the 'environment' that represents a timing signal from the original (user's) circuit design ." Defendant argues that the term "environmental timing signal" must (i) be periodic and have a fixed frequency, (ii) have a frequency that is lower than the internal clock frequency, and (iii) be sampled by the internal clock to produce a data input to the controller. The Court construes "**environmental timing signal**" as "a timing signal originating from the environment with a frequency that is lower than the internal clock frequency." ('176 Patent at 2:53.)

3. "Internal Clock", "Resynthesis"

Plaintiffs propose that "internal clock" simply "provides a time base for the resynthesized circuit's operation." Defendant construes "internal clock" to mean "a periodic signal of fixed frequency, existing within the configurable logic system and invisible to the environment, which provides the time base for scheduling the operation of the configurable logic system (i.e., the pipeline clock)." The Court incorporates elements from both constructions to construe the "**internal clock,**" or "virtual clock", as "a signal existing within the configurable logic system and invisible to the environment that provides a time base for

scheduling the operation of the resynthesized circuit." ('176 Patent at 2:53-54, 3:12-13, 4:37-40, Fig. 4A.)

The Court adopts Defendant's definition of "**resynthesis**" as "transforming a circuit design into a new design following an initial synthesis and analysis of the original circuit design."

4. "Buses"

Plaintiffs define "buses" as "an interface system to connect a number of devices." The Court adopts Defendant's construction of "**buses**" as "common electrical pathways between circuit elements" based on the language in the claims. ('176 Patent, Claims 8, 11.)

5. "Configuring the Logic System"

Defendant defines "configuring the logic system" to mean "implementing the logic within the configurable logic system to perform a desired logic operation or calculation." The Court adopts Plaintiffs' construction of "**configuring the logic system**" as "compiling and loading into a configurable logic system" based on the language in the claims and the specifications. ('176 Patent Claims 1 and 4, 1:31-33.)

6. "Control Signal", "Controller", "Controller Means"

Plaintiffs define "control signal" as "a signal that coordinates the application of logic operations." Defendant construes "control signal" to mean "an output from a controller that is used to dictate the operation of the sequential logic in the configurable logic system." The Court adopts a modified version of the Defendant's definition of "**control signal**" to mean "an output from a controller that is used to coordinate the operation of the sequential logic in the configurable logic system." ('176 Patent, 3:18-23, 3:26-27, 8:53-57.)

The Court construes "**controller**" or "**controller means**" to mean "a circuit configured into the logic system that coordinates the logic operations of the logic system in response to the internal clock signal and the environmental timing signal." Plaintiffs argue that a "controller" or "controller means" is "a circuit configured into the logic system capable of coordinating the logical operations of the logic system." Defendant argues that the definition must refer to "a finite state machine" that "dictates" operations "in response to an internal clock signal and a sampled environmental timing signal." The Court incorporates elements of both definitions into its construction, but rejects the specification of the "finite state machine", a preferred embodiment, into the definition based on the language of the claims and the specifications. ('176 Patent Claims 1-3, 12, 13, 27, 28, 40, at 3:7-10, 3:66-4:5.) The Court also finds persuasive Plaintiffs' argument that inclusion of the "finite state machine" language in the definition would render dependent Claim 3 redundant of independent Claim 1. ('176 Patent Claims 1-3.)

7. "Sampled", "Sampling"

Defendant construes "sampled" and "sampling" to mean "processed or processing at fixed, periodic intervals." The Court adopts Plaintiffs' construction of "**sampled**" and "**sampling**" as "the process by which a component (e.g., a state element) captures a signal value carried at a given point in time." ('176 Patent at 12:32-35.)

8. "Synchronize", "Synchronizer"

Defendant construes "synchronize" to mean "align a periodic signal to another periodic reference signal in

real time." The Court construes "**synchronize**" as "to make a version of a signal that is synchronous (i.e., has a defined timing relationship) with a reference signal." The Court further adopts Plaintiffs' construction of "**synchronizer**" as "a circuit for synchronizing." ('176 Patent at 9:55-60.)

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