United States District Court,
D. Delaware.

SILICON GRAPHICS, INC., a Delaware corporation,
Plaintiff.
v.
n VIDIA CORP., a California corporation,
Defendant.

Civil Action No. 98-188-RRM

June 24, 1999.

Owner of patent for computer graphics chip sued competitor for infringement. Construing claim language, the District Court, McKelvie, J., held that: (1) cache memory called for in claims had to store complete texture map; (2) requirement that functional elements be "coupled" to each other allowed connection of elements either directly or indirectly; (3) claim language did not preclude further on-chip processing of pixels in addition to texture mapping by interpolator; and (4) "interpolator" was something that interpolated.

Claims construed.

5,548,709, 5,706,481. Construed.

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Robert W. Whetzel and Jeffrey L. Moyer, Richards, Layton & Finger, Wilmington, DE; Stephen C. Neal, Tharan Gregory Lanier and Michelle Greer Galloway, Cooley Godward LLP, Palo Alto, CA; counsel for defendant.

OPINION

McKELVIE**, District Judge.**

This is a patent case. Silicon Graphics, Inc. alleges *n* Vidia Corporation is willfully infringing Silicon Graphics's patent, U.S. Patent No. 5,706,481. *n* Vidia denies liability and has counterclaimed for a declaratory judgment that the patent is invalid and not infringed. The case is scheduled to be tried to a jury beginning on July 12, 1999.

On May 25, 1999, in accordance with Markman v. Westview Instruments, Inc., 517 U.S. 370, 116 S.Ct. 1384, 134 L.Ed.2d 577 (1996), the court held the part of the trial necessary to construe the disputed terms of

the patent's claims. This is the court's decision on the construction of those terms.

I. *FACTUAL AND PROCEDURAL BACKGROUND*

The court draws the following facts from the Joint Pretrial Order, expert witness declarations submitted by the parties in connection with their summary judgment motions, and the documents offered into evidence by the parties, including the patent and its file history.

A. *The Parties*

Silicon Graphics, Inc. is a Delaware corporation with its principal place of business in Mountain View, California. It designs, develops, markets and sells computer hardware products, including products for generating three-dimensional ("3-D") computer graphics.

n Vidia is a Delaware corporation with its principal place of business in Sunnyvale, California. It designs, develops, markets and sells 3-D graphics processors for personal computers ("PC").

U.S. Patent No. 5,706,481 ("the '481 patent") was issued to Marc R. Hannah and Michael B. Nagy on August 20, 1997. Hannah and Nagy assigned it to Silicon Graphics. The '481 patent discloses a method for performing texture mapping and a computer system having a semiconductor chip for performing texture mapping.

In its complaint, Silicon Graphics alleges *n* Vidia infringes Claims 1-4 and 10-13 of the '481 patent by selling RIVA 128, RIVA 128ZX, RIVA TNT, TNT2, and VANTA graphics processor chips that can be added to a personal computer ("PC"), thus enabling a standard PC to produce 3-D graphics.

B. *Background on the Technology*

Computer systems are commonly used for displaying graphical objects on a display screen. The purpose of 3-D computer graphics is to create a two-dimensional image on a computer screen that realistically represents an object or objects in three-dimensions. Images created with 3-D computer graphics are used in a wide range of applications from video entertainment games to aircraft flight simulators, to portray in a realistic manner an individual's view of a scene at a given point in time. Well-known examples of 3-D computer graphics include special effects in Hollywood films such as *Terminator II* and *Jurassic Park*.

In the real world, objects occupy three dimensions. They have a real height, a real width and a real depth. A photograph is an example of a two-dimensional representation of a 3-D space. 3-D computer graphics are like a photograph in that they represent a 3-D world on the two-dimensional space of a computer screen.

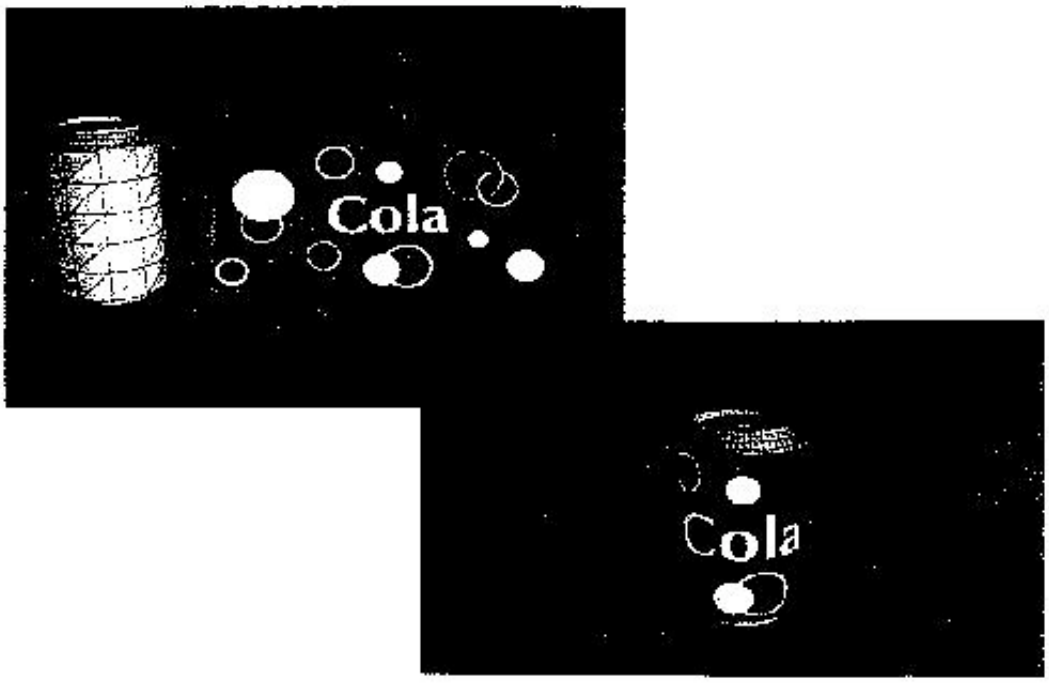
To create a 3-D computer graphical representation, the first step is to represent the objects to be depicted as mathematical models within the computer. 3-D models are made up of geometric points within a coordinate system consisting of an x, y and z axis; these axes correspond to width, height, and depth respectively. Objects are defined by a series of points, called vertices. The location of a point, or vertex, is defined by its x, y and z coordinates. When three or more of these points are connected, a polygon is formed. The simplest polygon is a triangle.

3-D shapes are created by connecting a number of two-dimensional polygons. Curved surfaces are represented by connecting many small polygons. The view of a 3-D shape composed of polygon outlines is

called a wire frame view. In sum, the computer creates 3-D objects by connecting a number of two-dimensional polygons.

To make the rendered 3-D objects appear more realistic, surface texture can be applied to the wire frame model in a process known as texture mapping. Silicon Graphics describes texture mapping as "the complex process of applying a two-dimensional texture or pattern to a three-dimensional object, so as to define detail, motion, and spatial cues (among other things) that are critical to a realistic rendering of objects in three-dimensional space." In other words, texture mapping is applying texture to a geometric object to make it look real.

A texture map represents the surface pattern of an object. It is made up of many small points of color. Silicon Graphics calls these "texels" or texture elements. Together, the texels define the surface pattern. To visualize how the surface texture is applied, one can imagine the texture map is a virtual wallpaper or contact paper bearing a design or pattern. The paper is "wrapped around" the 3-D wire frame geometric form. An example of texture mapping referred to in the specification of the '481 patent is a texture map defining a wood grain pattern that is mapped onto the outline of a featureless cube to create the appearance of a wood block. An example offered by the parties and illustrated below is an advertising display wrapped around the model of a can to depict a soda can.



When texture data is used by an application in a typical 3-D graphics system, the data is retrieved from a hard disk drive, CD-ROM or other mass storage device and loaded into the computer's main memory, which is located on one or more semiconductorchips. Texture data is sent via a data bus to an interpolator, which is a processor dedicated to translating the texture data into pixels, or picture elements. Pixels are the smallest

unit of color that can appear on a computer screen. The interpolator translates texture data into pixels by assigning a value to each pixel based upon the texture data. Further processing of the pixel value may occur to create effects such as lighting and fogging. Ultimately, the pixel is displayed on the computer screen as a unit of color. When the different colored pixels are viewed together on the computer screen, they represent the geometric form which has been "wrapped" in texture data.

C. *The* '481 Patent

The '481 patent is entitled "Apparatus and Method for Integrating Texture Memory and Interpolation Logic in a Computer System." The invention of the patent pertains to a semiconductor chip used in computer systems for performing texture mapping for graphics applications. U.S. Patent No. 5,706,481, col. 2, ll. 40-43.

The specification of the '481 patent identifies a problem in the design of previous texture mapping systems; essentially transferring texture data from one semiconductor chip to another one housing the interpolator would take up too much of the computer's resources for moving data. The specification states: "a problem is that the transfer of data between the various processors and the memory consumes a great deal of the limited bandwidth." Id. at col. 2, ll. 24-37. According to the specification, "[a]llocating valuable bandwidth for this function tends to slow down the exchange of other needed information. Hence, the overall effect is that this imposes a heavy burden on the texture mapping process." U.S. Patent Office No. 5,706,481, col. 2, ll. 24-37.

In its papers submitted to the court, Silicon Graphics offers the following explanation of the problem with texture mapping systems prior to the invention of the '481 patent. According to Silicon Graphics, whenever the interpolator needs texture data to output a pixel, that data is retrieved from the main memory located on a semiconductor chip and sent over the data bus to the interpolator on another semiconductor chip. Because an interpolator is capable of processing texture data faster than a data bus can transport it, the interpolator must wait for the data to be retrieved. Thus, the interpolator cannot operate at its peak efficiency. Furthermore, no other components of the computer system can travel on the data bus as texture data is conveyed.

The '481 patent solves this problem by placing a cache memory on the same semiconductor chip as the interpolator. The inventors call this chip a TRAM, which is an acronym for texture random access memory. A cache memory is a smaller and faster memory that stores small amounts of data at a location away from the main memory. In its papers submitted to the court, Silicon Graphics explains that by integrating a cache memory and a dedicated interpolator on a single semiconductor chip, the invention improves the speed and efficiency of the texture mapping operation.

In its papers submitted to the court, Silicon Graphics offers the following explanation of how the '481 patent's invention increases speed and efficiency. As texture data is retrieved from the main memory and is transported by the data bus to the interpolator for processing, the cache memory stores a copy of the texture data. There is a substantial likelihood that the information copied into the cache memory includes some of the texture data the interpolator needs to use to output the next pixel. Silicon Graphics refers to the pattern of re-using earlier retrieved texture mapping data as "locality of reference." The interpolator can quickly retrieve this nearby data instead of waiting for the same texture data to be transported from the main memory by the data bus. The cache memory can also retrieve and store texture data before the interpolator needs to process it. Because the interpolator does not need to contend with the limited bandwidth of the data

bus when using information stored in the cache memory, the interpolator is able to perform interpolation operations at a higher rate than if the information necessary to render each pixel were sent over the data bus. In this way, computer time and resources are saved.

The '481 patent has 18 claims. Claims 1 and 10 are independent claims. Claims 2-4 depend from Claim 1. Claims 11-13 depend from Claim 10. Claim 1 is an apparatus claim covering a semiconductor chip (TRAM). It includes four elements: (1) an input; (2) a cache memory coupled to the input; (3) an interpolator coupled to the cache memory; and (4) an output coupled to the interpolator. Claim 10 is a method claim covering the texture mapping process performed by a semiconductor chip (TRAM). It includes three elements: (1) storing texture mapping data in a cache memory; (2) interpolating texture mapping to produce an output rendered pixel; and (3) outputting an output rendered pixel.

Central to the parties' dispute is the nature of the cache memory described by Claims 1 and 10 of the '481 patent. In particular, the parties dispute whether the claims disclose a cache memory configured to store a complete texture mapping.

D. ***Matters in Issue***

1. ***Pleadings***

In its complaint, Silicon Graphics contends that by manufacturing and selling its RIVA 128, RIVA 128ZX, RIVA TNT, TNT2 and VANTA graphics processor chips, *n* Vidia is infringing and is inducing others to infringe Claims 1-4 and 10-13. *n* Vidia denies it infringes or that it induces others to infringe the '481 patent's claims. In addition, *n* Vidia counterclaims that the claims in issue are invalid due to indefiniteness and for lack of enablement. *n* Vidia also counterclaims that the claims are invalid on the basis of anticipation and obviousness, for lack of adequate written description and as indefinite.

2. ***Motions***

n Vidia has moved for a summary judgment that it does not infringe. It contends that the phrase "texture mapping data" in Claims 1 and 10 should be read to require on-chip storage of a complete texture pattern. *n* Vidia argues that because its chips are not configured to store a complete texture map on the chip, it does not infringe. In addition, *n* Vidia contends the fourth element of Claim 1 requires an output that is coupled to the interpolator. *n* Vidia argues that because the outputs of the RIVA chips are not coupled to the interpolators, it does not infringe.

Silicon Graphics has moved for a summary judgment of literal infringement. In support of its motion, it argues that the court should reject *n* Vidia's proposed claim constructions and the limitations *n* Vidia would add to the claims that the texture map must be a "complete" texture map, and that "coupled" means "directly connected." Silicon Graphics argues that once the court rejects these limitations, it is entitled to a summary judgment that *n* Vidia's chips literally infringe Claims 1-4 and 10-13 of the '481 patent.

n Vidia has also moved for summary judgment that Claims 1 and 10 are invalid as anticipated, as obvious, for lack of adequate written description and as indefinite. In support if its motion that the '481 patent is invalid as anticipated and obvious, it argues that the court should reject the limitation Silicon Graphics would add to the claims that the interpolator be "dedicated" or a "specific device."

3. ***Claim Construction***

The parties dispute the meaning of several of the terms in Claims 1 and 10 of the patent: (1) cache memory; (2) output rendered pixel; (3) coupled; and (4) interpolator.

Regarding the meaning of cache memory, Silicon Graphics contends that the court should use the plain meaning of the terms. *n* Vidia contends that read within the context of the prosecution history of the '481 patent and its parent application, cache memory should be construed to mean a cache memory configured to store a complete texture mapping.

E. ***The Prosecution History***

The court draws the following facts from the '481 patent and its prosecution history. In particular, the court looks to the prosecution history of the '481 patent and the patent which issued from the parent application of the '481 patent, U.S. Patent No. 5,548,709 ("the '709 patent").

1. ***Prosecution of*** the '709 Patent

On March 7, 1994, Marc R. Hannah and Michael D. Nagy filed Application No. 8/206,959 ("the '959 application") with the Patent and Trademark Office ("PTO"). As first filed, the application contained 19 pending claims, including Claim 19, which claims a TRAM comprising an interpolator and a cache memory. Claim 19 read:

A single semiconductor chip comprising a cache memory for storing texture information and an interpolator for generating a texel by interpolation from said texture information stored in said cache memory, wherein said cache memory and said interpolator both reside on said single semiconductor chip.

The other claims pertain to a TRAM including an on-chip main memory in addition to the elements recited by Claim 19.

On March 21, 1995, the PTO rejected pending Claims 1, 4, 10, 13 and 19 in the '959 application, as being anticipated or obvious in light of an article by Tom Williams on Intel's 80860 chip, entitled "80860 May Force Rethinking of Graphics System Architectures," *Computer Design,* 28:42 (July 1, 1989) ("the Williams 80860 reference"). In rejecting the pending claims, the examiner stated:

As per claims 1 and 19, Williams teaches that Intel's 80860 RISC-based 64-bit microprocessor chip contains a memory management unit, data and instruction caches, and pixel-generated circuitry for shaded 3D graphics. Williams further teaches that the 80860 graphics section contains interpolation and adder logic for rendering shaded triangles. And Williams teaches that the 80860 is used for texture mapping. Memory and I/O [in/out] are inherent features of any microprocessor design therefore the 80860 would have main memory as well as I/O.

(Citations omitted).

On June 29, 1995, the applicants responded to the rejection over the Williams 80860 reference, arguing there were differences between the pending claims in the '959 application and the Williams 80860 reference. Regarding the rejection of pending Claims 1, 10 and 19, the applicants contended in full:

Williams describes the Intel 80860 microprocessor ("80860") as having on-chip graphics processing

circuitry. Although the 80860 is capable of texture mapping, it does not have the specialized architecture found in the present invention. In particular, the graphics processor in the 80860 does not have a dedicated memory unit which can store a texture pattern, in contrast to the TRAM in the present invention. Although the Examiner is correct in stating that memory and I/O are inherent features of any microprocessor design, the present invention is clearly not a microprocessor. *Indeed, the on-chip TRAM of the present invention is designed to receive and store a complete texture pattern, whereas the 80860 would have to access off chip memory containing the texture pattern*. There is no indication that the data cache alone in the 80860 is suitable for holding a texture pattern. As a result, the texture mapping capability of the present invention would be superior to that of the 80860 because of fewer off chip memory accesses. Therefore, since the TRAM of the present invention or an equivalent is not found in the 80860 as described by Williams, Applicants respectfully request reconsideration and withdrawal of the rejection of claims 1, 10 and 19 under 35 U.S.C. s. 102.

(Emphasis added).

On October 20, 1995, the PTO issued an examiner action allowing Claims 1-18 of the '959 application and rejecting Claim 19. In allowing Claims 1-18 over the Williams 80860 reference, the examiner stated in full:

In view of the Applicant's remarks [contained in the June 26, 1995 response], the totality of the structural combinations recited is not rendered obvious by the prior art. Specifically, the cited prior art [Williams 80860 reference] does not teach a dedicated memory unit for storing a texture pattern, fault prediction means comprising more than cache miss notification as per the specification on pg. 15, lines 3-12, parallel memory access scheme, generating interpolations for different data widths, using interpolation schemes together on a single ic chip, and that filtering and pattern storage be done on a single chip.

In rejecting Claim 19 as anticipated by the Williams 80860 reference, the examiner stated in full:

As per claim 19, Williams teaches that Intel's 80860 RISC-based 64-bit microprocessor chip contains a memory management unit, data and instruction caches, and pixel-generated circuitry for shaded 3D graphics. Williams further teaches that the 80860 graphics section contains interpolation and adder logic for rendering shaded triangles. And Williams teaches that the 80860 is used for texture mapping.

(Citations omitted).

On January 16, 1996, the applicants canceled Claim 19, and on February 14, 1996, the PTO issued a notice of allowability for Claims 1-18 of the '959 application, which issued as U.S. Patent No. 5,548,709 ("the '709 patent"). The inventors assigned the patent to Silicon Graphics.

Like the '481 patent, the '709 patent discloses a semiconductor chip used to perform texture mapping and a method of performing texture mapping. The invention claims a chip containing a main memory, a cache memory, an interpolator, and a memory controller which controls the data transfers between the main memory and the cache memory. The invention differs from the invention of the '481 patent in that the '709 patent claims a chip containing a memory controller and a main memory on the chip. The '481 patent does not claim a memory controller or a main memory that is on the chip containing the interpolator and the cache memory.

The '709 patent has 18 claims. Claims 1 and 10 are independent claims. Claim 1 is an apparatus claim

covering a semiconductor chip (TRAM). It includes six elements: (1) an input; (2) a main memory coupled to the input; (3) a cache memory coupled to the main memory; (4) a memory controller coupled to the main memory and cache memory; (5) an interpolator coupled to the main memory and cache memory; and (6) an output coupled to the interpolator. Claim 1 reads as follows:

Claim 1

In a computer system, a semiconductor chip for performing texture mapping, said semiconductor chip comprising:
an input for inputting textures to said semiconductor chip;

a main memory coupled to said input for storing said textures;

a cache memory coupled to said main memory, for storing recently used textures;

a memory controller coupled to said main memory and said cache memory for controlling data transfers between said main memory and said cache memory;

an interpolator coupled to said main memory and said cache memory for producing an output rendered pixel by interpolating from said recently used textures stored in said cache memory;

an output coupled to said interpolator for outputting said output rendered pixel, wherein said input, said main memory, said cache memory, said memory controller, and said interpolator reside on a single substrate.

Claim 10 is a method claim covering the texture mapping process performed by a semiconductor chip (TRAM). It includes six elements: (1) inputting textures; (2) storing textures in a main memory; (3) storing recently used textures in a cache memory; (4) controlling data transfer; (5) interpolating from recently used texture to produce an output rendered pixel; and (3) outputting an output rendered pixel. Claim 10 reads as follows:

Claim 10

In a computer system, a method of performing texture mapping, said method comprising the steps of:
inputting textures to a semiconductor chip;

storing said textures in a main memory of said semiconductor chip;

storing a recently used texture in a cache memory of said semiconductor chip;

controlling data transfers between said main memory and said cache memory;

producing an output rendered pixel by implementing an interpolator and interpolating from said recently used texture stored in said cache memory, wherein said interpolator resides on said semiconductor chip;

outputting said output rendered pixel from said semiconductor chip.

2. *Prosecution of* the '481 Patent

On May 22, 1996, Hannah and Nagy filed Application No. 08/206,117 ("the '117 application"), as a continuation of the '959 application. When first filed, the '117 application contained the specification and the original 19 claims of the '959 application. On November 5, 1996, the applicants filed an amendment, canceling pending Claims 1-19, and adding pending Claims 20-37. These claims are related to the '959 application's Claim 19. Both Claim 19 of the '959 application and Claims 20-37 of the '117 application disclose a semiconductor chip comprising a cache memory and an interpolator, but not an on-chip main memory, which is an element of the claims of the '709 patent.

In the remarks section of the preliminary amendment, Silicon Graphics made the following representations concerning the then pending claims:

The present invention is directed at a semiconductor integrated circuit chip which is dedicated to graphics processing, and in particular, texture mapping. For example, Independent Claims 20 and 29 include the unique limitation of a cache memory and an interpolator residing on the semiconductor chip dedicated to texture mapping, *wherein the cache memory is configured to store a complete texture mapping*.

While prosecuting the parent application, several related claims had been rejected as being anticipated by the article by Williams [the Williams 80860 reference].

Williams describes the Intel 80860 microprocessor ("80860") as having on-chip graphics processing circuitry. *Although the 80860 is capable of texture mapping, it does not have the specialized architecture as claimed by applicants. In particular, the graphics processor in the 80860 does not have a cache memory that, alone, is capable of holding a complete texture pattern*.

The present invention as claimed, however, includes the structural limitation of *having a cache memory that is configured to store a complete texture mapping*. As a result, the texture mapping capability of the present invention would be superior to that of the 80860 because fewer off chip memory accesses would be necessary.

(Emphasis added) (Citations omitted).

The applicants stated in conclusion:

Therefore, since the unique combination of a semiconductor chip dedicated to graphics processing having a cache memory that is configured to store a complete texture mapping, so as to require less memory accesses off chip, is not disclosed or suggested by any of the cited prior art references, applicants respectfully submit the claimed invention is in condition for allowance.

In a January 14, 1997 office action, the examiner rejected pending Claims 20-37 for obviousness-type double patenting, and rejected pending Claims 20-28 as indefinite under 35 U.S.C. s. 112, second paragraph.

In the remarks accompanying this action regarding the double patenting rejection, the examiner compared Claims 1 and 2 of the '709 patent with pending Claims 20 and 21 of the '117 application. The examiner found that Claims 1 and 2 of the '709 patent differ from pending Claims 20 and 21 "in that [the '709 patent] claims 'an input for inputting textures to said semiconductor chip,' a 'main memory ... for storing said textures,' and 'a memory controller' in addition to all of the elements of claims 20 and 21 of this application." The examiner found the only differences between the inventions of the '709 patent and the '117

application were as follows:

1) an input to the semiconductor chip is recited in [the '709 patent] and not in this application, 2) the cache memory of this application is recited to store "a complete texture mapping" whereas the cache memory of [the '709 patent] is recited to store "a recently used texture[,]" and 3) the main memory is disposed on the chip in [the '709 patent] and off the chip in this application.

With respect to the second enumerated difference, the examiner observed:

since both caches store texture map data, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have stored in the cache [ ] "a recently used texture" in place of [ ] "a complete texture mapping" to facilitate a type of texture processing desired.

The examiner compared pending Claim 29 to the '709 patent's Claims 10 and 11. The examiner found Claims 10 and 11 of the '709 patent differ from pending Claims 29 and 30 "in that [the '709 patent] claims 'inputting textures to a semiconductor chip,' [ ] 'storing said textures in main memory ...' [ ] and 'controlling data transfers between said main memory and said cache memory' in addition to all of the steps of claims 29 and 30 of this application." The examiner found the only differences between the inventions are as follows:

1) inputting textures to the chip in [the '709 patent]; 2) storing the textures in the main memory on the chip in [the '709 patent]; and 3) storing a recently used texture in the cache in [the '709 patent] and a complete texture mapping in the cache in this application.

With respect to the second enumerated difference, the examiner observed:

since both caches store texture map data, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have stored in the cache a "recently used texture" in place of [ ] "a complete texture mapping" to facilitate the type of texture processing desired.

On April 29, 1997, the applicants also filed an amendment. The applicants amended pending Claims 20 and 29 by deleting the term "complete texture mapping" and inserting "texture mapping data" in its place. The applicants also amended Claim 20 to require "an input configured to input texture mappings to said semiconductor." The applicants stated that they had submitted a Terminal Disclaimer to overcome the examiner's rejectionfor obviousness-type double patenting over the '709 patent. The applicants also stated: "Applicants have amended claims 20 and 29 in response to the Examiner's rejection under 35 U.S.C. s. 112 second paragraph. Moreover, the claims have been amended to more accurately claim the operations of the present invention."

On April 30, 1997, the applicants filed a Terminal Disclaimer agreeing that any patent issuing from the '117 application would only be enforceable for the statutory term of the '709 patent.

On August 20, 1997, the PTO issued a notice of allowability, allowing the '117 application's pending Claims 20-37, which issued as the '481 patent's Claims 1-18. The inventors assigned the patent to Silicon Graphics.

The parties' claim construction disputes concern terms in the '481 patent's independent claims, Claims 1 and 10, which are the same as the '117 application's pending Claims 20 and 29, respectively. Claim 1 of the '481 patent reads as follows, with disputed phrases italicized:

Claim 1

A computer system having semiconductor chip for performing texture mapping, said semiconductor chip comprising:
an input configured to input texture mappings to said semiconductor chip;

a *cache memory coupled* to said input, said *cache memory configured to store texture mapping data;*

an *interpolator coupled* to said *cache memory* for producing an output rendered pixel by interpolating from a texture mapping stored in said *cache memory;* and

an *output coupled to said interpolator for outputting said output rendered pixel,* wherein said input, said *cache memory,* and said *interpolator* reside on a single substrate device.

Claim 10 of the '481 patent reads as follows, with disputed phrases italicized:
Claim 10

A method for performing texture mapping, said method comprising the steps of:
storing texture mapping data on a cache memory residing on a semiconductor chip;

producing an output rendered pixel via an *interpolator* interpolating from a texture mapping stored in said *cache memory,* said *interpolator* residing on said semiconductor chip; and

outputting said output rendered pixel from said semiconductor chip.

II. DISCUSSION

Based upon the above findings, the court construes the meanings of the disputed terms of the '481 patent.

A. *Claim Construction*

1. *What is the Legal Standard Under Which the Court Construes the Patent Claims?*

[1] [2] [3] [4] [5] Claim construction is a matter for the court. Markman v. Westview Instruments, Inc., 52 F.3d 967, 979 (Fed.Cir.1995) (*en banc*), *aff'd,* 517 U.S. 370, 116 S.Ct. 1384, 134 L.Ed.2d 577 (1996). The court construes claims according to their "ordinary and accustomed meaning." *See* Renishaw PLC v. Marposs Societa per Azioni, 158 F.3d 1243, 1249 (Fed.Cir.1998). Claims are construed from the vantage point of a person of ordinary skill in the art at the time of the invention. Markman, 52 F.3d at 986. In construing a claim, a court looks first to the intrinsic evidence of record, namely, the language of the claim, the specification, and the prosecution history. Insituform Technologies, Inc. v. Cat Contracting, Inc., 99 F.3d 1098, 1105 (Fed.Cir.1996), *cert. denied,* 520 U.S. 1198, 117 S.Ct. 1555, 137 L.Ed.2d 703 (1997). The claim language itself defines the scope of the claim, and "a construing court does not accord the specification, prosecution history, and other relevant evidencethe same weight as the claims themselves, but consults these sources to give the necessary context to the claim language." Eastman Kodak Co. v. Goodyear Tire & Rubber Co., 114 F.3d 1547, 1552 (Fed.Cir.1997).

[6] Although extrinsic evidence such as expert testimony may be considered if needed to assist the court in

understanding the technology at issue or in determining the meaning or scope of technical terms in a claim, Hoechst Celanese Corp. v. BP Chems. Ltd., 78 F.3d 1575, 1579 (Fed.Cir.), *cert. denied,* 519 U.S. 911, 117 S.Ct. 275, 136 L.Ed.2d 198 (1996), reliance on any extrinsic evidence is improper where the public record, *i.e.,* the claims, specification, and file history, unambiguously defines the scope of the claims. Vitronics Corp. v. Conceptronic, Inc., 90 F.3d 1576, 1583 (Fed.Cir.1996).

2. ***What is the Proper Construction of the Phrases "Cache Memory Configured to Store Texture Mapping Data" and "Storing Texture Mapping Data on a Cache Memory" in Claims 1 and 10 of*** the '481 Patent***?***

The parties dispute whether the phrases "a cache memory configured to store texture mapping data" in Claim 1 and "storing texture mapping data on a cache memory" in Claim 10 require a cache memory that stores a complete texture map. *n* Vidia contends they do. Silicon Graphics contends they do not.

According to Silicon Graphics, the plain language of the claims does not require a cache memory configured to store a complete texture map, but only one configured to store "data" used for "texture mapping."

n Vidia makes several arguments in support of its proposed claim construction. Each is based on the statements the applicants made to the examiner in the course of presenting their applications for the '709 and '481 patents. First, *n* Vidia contends with these statements the applicants acted as their own lexicographers in describing and defining the cache memory and adopted a definition that it is a memory configured to store a complete texture mapping. Second, *n* Vidia contends that by these statements the applicants disclaimed any meaning for the cache memory other than one that would store a complete texture pattern. Third, *n* Vidia contends that the court should avoid construing the cache memory as configured to store less than a complete texture map, as that would render the claims obvious in light of the Williams 80860 reference.

a. ***Did the applicants act as their own lexicographers and define the phrase "cache memory" to mean a cache memory configured to store a complete texture mapping?***

As a starting point, the court agrees that the plain meaning of the words in Claims 1 and 10 do not appear to describe a cache memory configured to store a complete texture mapping. Normally, the words "texture mapping data" read to suggest that the cache is configured to store some data, but not necessarily all or a complete texture mapping.

[7] *n* Vidia's position depends, therefore, on whether it can demonstrate that the applicants had used these words to express something other than their ordinary meaning. The Federal Circuit teaches that a term in a claim can be given something other than its ordinary and accustomed meaning when the patentee has chosen to be his own lexicographer "by clearly setting forth an explicit definition for a claim term." Johnson Worldwide Assoc., Inc. v. Zebco Corporation, 175 F.3d 985, 1999 WL 243570, (Fed.Cir. April 27, 1999).

In this case, the court has four critical facts before it. First, in prosecuting both the '481 and '709 patents and in distinguishing their invention from the prior art, the applicants described the specialized architecture of their invention as including an on-chip TRAM designed to receive and store a complete texture pattern or complete texture mapping. Second, after offering this description of their invention, the applicants amended the '481 patent's Claims 1 and 10 to delete the words "complete texture mapping" and inserted in their place the words "texture mapping data." Third, in amending Claims 1 and 10, the applicants reported to the examiner that "the claims have been amended to more accurately claim the operations of the present

invention." Fourth, Silicon Graphics now contends that the patent claims a cache memory that is not designed to receive and store a complete texture mapping.

While the second and fourth facts may be consistent with the words in Claims 1 and 10 if they are read according to their ordinary meaning, Silicon Graphics's current contention as to the architecture or configuration of the cache memory claimed is not consistent with the first and third facts. The question the court now addresses is what is the significance of the first and third facts? More precisely, can and should the inconsistency between the second and fourth facts and the first and third facts be resolved in the context of claim construction?

The court first notes that the Federal Circuit teaches "[c]ommon words, unless the context suggests otherwise, should be interpreted according to their ordinary meaning." Desper Products, Inc. v. QSound Labs, Inc., 157 F.3d 1325, 1336 (Fed.Cir.1998). In *Desper Products,* the Federal Circuit interpreted the term "prior to" according to the "context of the specification." *Id.*

Silicon Graphics urges the court to approach any inconsistency between their statements concerning the Williams 80860 reference and the claims as an obviousness issue. The court, however, is inclined to find that this is, at least in part, a matter that can be resolved in the context of claim construction.

Prosecution history is an important source of intrinsic evidence in interpreting claims because it is a contemporaneous exchange between the applicant and the examiner. *Id.* at 1336-37. Starting with the prosecution history of the '709 patent, we see that in distinguishing pending Claims 1, 10 and 19 from the Williams 80860 reference, the applicants represented that a distinctive feature of the invention is that the "on-chip TRAM of the present invention is designed to receive and store a complete texture pattern." Pending Claim 19 claims a TRAM with only a cache memory for storing texture information. In the context of pending Claim 19, the applicants' statement must mean that the cache memory "is designed to receive and store a complete texture pattern."

The applicants subsequently canceled pending Claim 19. When the applicants refiled their application as the '117 application, they based pending Claims 20 and 29 on the '959 application's pending Claim 19; all three claims claimed a TRAM containing a cache memory and an interpolator, and all three claims do not claim an on-chip main memory. When presenting these claims to the examiner, the applicants claimed as a specific structural limitation an equivalent limitation to the one they placed on pending Claim 19 to distinguish it from the prior art: a cache memory that is configured to store a complete texture mapping.

Next, the examiner rejected Claims 1 and 10 for double patenting in light of the '709 patent. In explaining the action, the examiner referred to the phrase "complete texture mapping" in the '117 application as one of three differences in the claims of the two inventions. The examiner then discounted this distinction, finding it would have been obvious to store "a recently used texture" in the cache memory in place of "a complete texture mapping." This latter statement by the examiner is somewhat confusing, because the examiner appears to have inverted the chronology of the patents by stating that storing "a recently used texture" would be obvious in place of storing "a complete texture mapping."

[8] The applicants overcame the double patenting rejection by filing a terminal disclaimer agreeing that any patent that issued from the '117 application would have the same statutory term of protection as the '709 patent. A terminal disclaimer is a technical and procedural device that allows inventors to incorporate later developments into their original patents without violating the double-patenting bar. 35 U.S.C. s. 253.

The applicants also amended pending Claims 20 and 29, replacing the phrase "complete texture mapping" with the phrase "texture mapping data." Silicon Graphics now argues the applicants took the opportunity to disclaim the "complete texture mapping" limitation.

The applicant's amendment could have been a significant change in the invention they were claiming, if they did not already define "cache memory" to mean a cache memory configured to store a complete texture mapping, or give the same meaning to the phrase "complete texture mapping" as to "texture mapping data." This change would have been significant in such a case both because it would have deleted what the applicants had previously described as a unique aspect of their invention, and because it would have sought to capture or recapture a structure they had specifically disclaimed.

One would expect that, if the applicants had intended these significant changes, they would have so stated and would have identified their intention to the examiner. They did not. Instead, the applicants explained to the examiner that they had amended their claims "to more accurately claim the operations of the present invention." If that statement is correct, then it must be that the applicants had not intended the amendment to make a significant change in the description of their invention and in the matters claimed. Accordingly, if that statement is correct, and the amendments were nothing more than an attempt to "more accurately" claim the operations of the claimed invention, then we should read them so that they "more accurately" claim the invention.

The applicants have previously described their invention as "having a cache memory that is configured to store a complete texture mapping." It would not be a more accurate description of the invention to withdraw from the invention the structural limitation that the cache memory be configured to store a complete texture mapping, which the applicants have previously stated is one of the unique aspects of their invention. The applicants relied on this distinction in the '117 and '959 applications to distinguish their invention from prior art. Disclaiming it would have required an explanation as to how the invention overcame the prior art Williams 80860 reference.

It must be, then, that by stating that they were providing a more accurate description of their invention, the applicants did not intend to contradict their prior description, but to add precision to it. Accordingly, the applicants must have believed that the phrase "texture mapping data" added precision to their claims, while, at the same time, maintained the structural limitation that the cache memory be configured to store a complete texture mapping.

The applicants' representations throughout the course of the prosecution history demonstrate that the applicants acted as their own lexicographers in defining the phrase "cache memory." While prosecuting the '959 application, the applicants represented that the cache memory claimed in pending Claim 19 was designed to store a complete texture pattern, even though the claim did not contain the phrase "complete texture pattern" or the term "complete." Instead, the applicants acted as their own lexicographers to define cache memory to mean something different than its ordinary meaning. The applicants retained their own definition of the phrase "cache memory" when prosecuting the '481 patent by representing pending Claims 20 and 29 of the '117 application were configured to store complete mapping data. Even when the applicants dropped the words "complete mapping data" out of the claim, this did not remove the structural limitation, because the stated reason for the amendment was to "more accurately claim the operations of the present invention."

[9] In this context, the court finds that the applicants have acted as their own lexicographers. The applicants clearly set forth an explicit definition of the phrase "cache memory" in Claims 1 and 10 of the '481 patent. *See* Johnson Worldwide Assoc., Inc. v. Zebco Corporation, 175 F.3d 985, 989-90. It is apparent from the applicants' statements that they intended to use the phrase "texture mapping" consistently with the phrase "complete texture mapping" so as to define the cache memory as configured to store a complete texture map. The public had a right to rely on the applicant's representations during the prosecution history. *See* Spectrum Int'l, Inc. v. Sterilite Corp., 164 F.3d 1372, 1378 (Fed.Cir.1998); Digital Biometrics, Inc. v. Identix, Inc., 149 F.3d 1335, 1347 (Fed.Cir.1998) ("The public has a right to rely on such definitive statements made during prosecution. Notice is an important function of the patent prosecution process ....").

Accordingly, the court construes the phrase "cache memory" in Claims 1 and 10 of the '481 patent to mean a cache memory configured to store a complete texture mapping.

b. ***Did the applicants disclaim a chip that stores less than a complete texture pattern in on-chip memory?***

Because the court has found that the applicants acted as their own lexicographers by defining cache memory to mean a cache memory designed to store a "complete texture mapping," the court need not reach the issue of whether the applicants disclaimed a chip that stores less than a complete texture pattern in on-chip memory.

c. ***Is it proper for the court to interpret "cache memory" as meaning anything other than a cache memory configured to store a complete texture mapping?***

n Vidia argues that Silicon Graphics's proposed construction results in Claims 1 and 10 of the '481 patent being as broad as the '959 application's Claim 19, which the examiner rejected based on prior art, and which the applicants canceled. *n* Vidia argues that the court should not adopt a meaning of the phrase "texture mapping data" which would invalidate the '481 patent. Because the court has found that the phrase "texture mapping data" in Claims 1 and 10 of the '481 patent means "complete texture mapping," the court need not reach this issue.

3. ***What is the Proper Construction of the Term "Coupled" in Claim 1 of*** the '481 Patent***?***

[10] Claim 1 of the '481 patent uses the term "coupled." Silicon Graphics contends the term "coupled" requires that the specified components be coupled or connected, directly or indirectly. This would encompass any electrical connection that allows a signal to travel from one circuit to another, whether directly or indirectly. *n* Vidia contends the term "coupled" means "directly coupled" or "directly connected." Under *n* Vidia's proposed construction, "coupled" would include, for example, a wire between points A and B with no other components in between.

Neither the claim nor the specification defines the term "coupled." Both parties refer to dictionary definitions to support their proposed constructions. For example, Silicon Graphics cites a technical dictionary of electronics, which defines the term "couple" as "to connect two circuits so signals are transferred from one to the other." Sclater, N. and Markus, J., *McGraw-Hill Electronics Dictionary* (6th Ed.1997). *n* Vidia counters with definitions of "couple" that include: (1) "to link together; connect," from *The American Heritage College Dictionary,* (3d Ed.) at 318; and (2) "a rather vague term, used to indicate that systems which might operate separately are actually being used in some form of cooperative mode...." from the *Dictionary of Computing,* (4th Ed.1996)

The Federal Circuit teaches that "a court must presume that the terms in the claim mean what they say, and, unless otherwise compelled, give full effect to the ordinary and accustomed meaning of claim terms." Johnson Worldwide Associates, Inc. v. Zebco Corp., 175 F.3d 985, 1999 WL 243570, *3; *see also* Hoganas AB v. Dresser Industries, Inc., 9 F.3d 948, 951 (Fed.Cir.1993) ("Although a patentee can be his own lexicographer, as we have repeatedly said, the words of a claim 'will be given their ordinary meaning, unless it appears that the inventor used them differently.' "); Intellicall, Inc. v. Phonometrics, Inc., 952 F.2d 1384, 1387 (Fed.Cir.1992). The court notes that the ordinary and accustomed meaning of the term "couple," even when used in an electronics context does not solely mean "directly coupled."

The specification of the '481 patent sheds some light on the meaning of "coupled." For example, Claim 1 recites that the cache is coupled to the input. Figure 2 is a block diagram of a TRAM as an embodiment of the inventions claimed in the patent. In this diagram, the cache is not directly connected to the input line, instead there is a DRAM array and an input buffer between the cache and input line. This arrangement suggests that "coupled" means directly or indirectly connected.

The specification and claims of the '709 patent also support this construction. Claim 1 of the '709 patent recites "an interpolator coupled to said main memory and said cache memory." Figure 2 of the specification is a diagram similar to Figure 2 of the '481 patent that shows the interpolator directly connected to the cache but not to the main memory. The Federal Circuit teaches that the prosecution history of a parent application may be considered by the court in its interpretation. *See, e.g.,* Abtox, Inc. v. Exitron Corp., 122 F.3d 1019, 1027 (Fed.Cir.) *modified,* 131 F.3d 1009 (Fed.Cir.1997) (noting statements in the parent application may be considered but must be confined to their proper context). The Federal Circuit has explained that an inventor is not likely to define the invention in a way that excludes the preferred embodiment. Hoechst Celanese Corp. v. BP Chemicals, Ltd., 78 F.3d at 1581.

The court finds no reason not to apply the ordinary meaning of the term "couple," and determines that the ordinary meaning in this context is "coupled or connected, directly or indirectly."

4. *What is the Proper Construction of the Phrase "An Output Coupled to Said Interpolator for Outputting Said Output Rendered Pixel" in Claim 1 of* the '481 Patent ***and "Outputting Said Output Rendered Pixel from Said Semiconductor Chip" in Claim 10 of*** the '481 Patent***?***

Claim 1 of the '481 patent states "an output coupled to said interpolator for outputting said output rendered pixel ...." Claim 10 of the '481 patent states "outputting said output rendered pixel from said semiconductor chip ...." The parties dispute the meaning of the terms "output," and "outputting" and "output rendered pixel."

All of *n* Vidia's arguments concerning the meaning of these terms flow from the underlying premise that the '481 patent does not claim further processing of the pixel on the semiconductor chip after the interpolator has performed its texture mapping functions and rendered a value. To support this position, *n* Vidia contends that outputting from the interpolator and from the semiconductor are one in the same, and that an output rendered pixel is the texture mapped pixel output by the interpolator that has not received further on-chip processing. *n* Vidia bases its argument upon statements made in the '481 patent's specification and the prosecution history.

Silicon Graphics, on the other hand, contends the phrases at issue can be understood according to the ordinary meaning of their terms. Silicon Graphics argues the phrase "an output coupled to said interpolator

for outputting said output rendered pixel" in Claim 1 describes an output and outputting from the interpolator, and not necessarily from the semiconductor. Similarly, Silicon Graphics contends the phrase "outputting said output rendered pixel from said semiconductor chip" in Claim 10 describes outputting from the semiconductor, and not necessarily from the interpolator. Silicon Graphics also argues the claims encompass other on-chip processing in addition to texture mapping.

This claim construction dispute underlies the literal infringement dispute. *n* Vidia's allegedly infringing graphics chips perform processing in addition to mapping texture onto a pixel before outputting the pixel from the chip. For example, additional on-chip processing maps lighting and fogging effects on the pixel. According to Silicon Graphics's claim construction, a graphics chip which performs on-chip processing in addition to mapping texture onto the pixel may literally infringe Claims 1 and 10. According to *n* Vidia's interpretation, a chip which performs on-chip processing of a pixel after the pixel is output by the interpolator does not literally infringe either Claim 1 or Claim 10.

a. ***What is the meaning of the phrase "an output coupled to said interpolator for outputting said output rendered pixel" in Claim 1 of*** the '481 patent***?***

The plain language of Claim 1 does not suggest that outputting or the output from the interpolator must be the same as outputting or the output from the semiconductor chip. Neither does the claim language define "output rendered pixel" as a rendered pixel output from the semiconductor with no processing other than the texture mapping performed by the interpolator.

n Vidia argues that the inventors understood the output and outputting from the interpolator to be the same as the output and outputting from the semiconductor, and that they understood an "output rendered pixel" to be a texture mapped pixel that had not been further processed before being output by both the interpolator and the semiconductor. *n* Vidia cites the '481 patent' s "Summary of Invention," which states: "[a]lso included within the same semiconductor chip is one or more interpolators. These interpolators produce an output texel by interpolating from the textures stored in memory. The interpolated texel value is output by the semiconductor chip for display."

n Vidia argues that, based upon this understanding of the invention, the applicants limited the meaning of the term "output rendered pixel" during prosecution. During the prosecution of the '709 patent, the applicants amended pending Claims 1 and 19, replacing the word "texel" with the phrase "output rendered pixel." With respect to this amendment, the applicants stated: "[t]he word 'texel' as used in the claims refers to a pixel element of an object to which the texture pattern has been mapped, the pixel element being available at the chip's output as a 'rendered pixel.' "

These combined statements lead to the conclusion that the applicants understood that the pixel processed by the interpolator would be output from the semiconductor chip. These statements do not lead to the conclusion, however, that the inventors thought the patent did not disclose mapping additional data onto the pixel after the pixel is output from the interpolator but before the pixel is output from the semiconductor.

n Vidia argues the patent's specification discloses that the "output rendered pixel" undergoes further processing in addition to texture mapping only after being output from the TRAM. In support, *n* Vidia cites the specification, which reads: "[t]he pixel data is sent to the raster subsystem, whereupon the z-buffering, blending, texturing and anti-aliasing functions [additional processing functions] are performed. The resulting pixel values are stored in frame buffer 109. The display subsystem reads frame buffer and displays the

image on display monitor" U.S. Patent No. 5,706,481, col. 4, ll. 16-21.

[11] The language *n* Vidia cites refers to the specific example of a computer system utilizing the invention depicted in Figure 1 of the '481 patent. The Federal Circuit teaches that particular embodiments appearing in a specification should not be read into the claims when the claim language is broader than such embodiments. *See, e.g.,* Electro Medical Systems, S.A. v. Cooper Life Sciences, Inc., 34 F.3d 1048, 1054 (Fed.Cir.1994). Accordingly, the court finds that this statement does not disclaim processing on the TRAM in addition to the texture mapping performed by the interpolator.

[12] Because *n* Vidia has not demonstrated that the claim, specification, or prosecution history limits the meaning of the phrase at issue, the court construes it according to the ordinary meaning of its terms. Johnson Worldwide Associates, Inc. v. Zebco Corp., 175 F.3d 985, 1999 WL 243570, *3. The court finds the phrase "an output coupled to said interpolator for outputting said output rendered pixel" in Claim 1 of the '481 patent means an output coupled to the interpolator for outputting the output rendered pixel. The court finds that outputting the output rendered pixel from the interpolator, as described in Claim 1, does not have to be the same step as outputting the output rendered pixel from the semiconductor. The court also finds that an "output rendered pixel" may undergo further on-chip processing in addition to texture mapping.

b. *What is the meaning of the phrase "outputting said output rendered pixel from said semiconductor chip" in Claim 10 of* the '481 Patent***?***

The plain language of the claim does not suggest that outputting the output rendered pixel from the semiconductor chip must be the same step as outputting the output rendered pixel from the interpolator. Neither does the claim language define "output rendered pixel" as a pixel that the interpolator has mapped texture onto and that has not been further processed on-chip.

As discussed above, *n* Vidia has not demonstrated that the claims, specification or prosecution history limits the claim's meaning.

The court construes the phrase according to the ordinary meaning of its terms. Accordingly, the court construes the phrase "outputting said output rendered pixel from said semiconductor chip" in Claim 10 of the '481 Patent to mean outputting the output rendered pixel from the semiconductor chip. The court finds that outputting the output rendered pixel from the semiconductor, as described in Claim 10, does not have to be the same step as outputting the output rendered pixel from the interpolator. Also, the court finds that an "output rendered pixel" may undergo further on-chip processing in addition to texture mapping by the interpolator.

5. *What is the Proper Construction of the Term "Interpolator" in Claims 1 and 10 of* the '481 Patent***?***

Claims 1 and 10 of the '481 patent use the term "interpolator." *n* Vidia contends that the term "interpolator" should be interpreted according to the plain meaning of the term, and that it means something which interpolates. Silicon Graphics contends that interpolator means dedicated circuitry that performs interpolation, or a specific device within which the texture values to be assigned to pixels are calculated.

The '481 patent's specification provides a summary of the invention that states: "included within the same semiconductor chip [as the cache] is one or more interpolators. These interpolators produce an output texel by interpolating from the textures stored in memory." U.S. Patent No. 5,706,481, col. 2, ll. 47-50. The patent also describes the invention as "[a]n apparatus and method for integrating texture memory and interpolation

logic for performing texture mapping in a computer display system ...." Id. at col. 3, ll. 35-37.

[13] Neither the patent's specification, claims nor prosecution history provide support for Silicon Graphics's argument that the interpolator means either "dedicated circuitry" or "a specific device" for interpolating pixels. Accordingly, the court looks to the ordinary meaning of the term. Johnson Worldwide Associates, Inc. v. Zebco Corp., 175 F.3d 985, 1999 WL 243570, *3. The ordinary meaning of the term "interpolator" is to interpolate. *n* Vidia provides the definition for interpolate in *The American Heritage College Dictionary,* which is as follows: "4. *Math*. To estimate a value of (a function or series) between two known values." *The American Heritage College Dictionary,* 710 (3d Ed.).

The court construes the term "interpolator" according to its ordinary meaning, and finds the term means something which interpolates.

III. ***CONCLUSION***

The court construes the phrase "texture mapping data" in Claims 1 and 10 of the '481 patent to mean complete texture mapping. The court construes the term "coupled" in Claim 1 of the '481 patent to mean coupled or connected, directly or indirectly. The court construes the phrase "an output coupled to said interpolator for outputting said output rendered pixel" in Claim 1 of the '481 patent to mean an output coupled to the interpolator for outputting an output rendered pixel. The court construes the phrase "outputting said output rendered pixel from said semiconductor chip" in Claim 10 of the '481 patent to mean outputting an output rendered pixel from the semiconductor chip. The court construes the phrase "output rendered pixel" in Claims 1 and 10 of the '481 patent to mean a pixel to which texture data and any other data has been mapped. The court construes the term "interpolator" in Claims 1 and 10 of the '481 patent to mean something which interpolates.

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