United States District Court,
D. New Jersey.

GENERAL ELECTRIC COMPANY,
Plaintiff.
v.
NINTENDO COMPANY, LTD. and Nintendo of America, Inc,
Defendants.

Oct. 7, 1997.

As Amended Nov. 7, 1997.

Owner of patents relating to electronic circuitry used in connection with television systems brought infringement action against manufacturer of video game systems. Video game manufacturer moved for summary judgment. The District Court, Wolin, J., held that: (1) patent for video record player switching system was invalid as anticipated, and (2) patents were not infringed.

Defendant's motion for summary judgment granted.

4,282,549, 4,709,256. Cited.

Lisa M. Walsh, Tricia Bevelock O'Reilly, Marc D. Haefner, Connell, Foley & Geiser, Roseland, NJ and Thomas V. Heyman, Joseph D. Pollack, Blaney Harper, Douglas I. Lewis, Jones, Day, Reavis & Pogue, New York, NY, for Plaintiff.

John J. Kirby, Jr, Thomas G. Gallatin, Jr., Robert J. Gunther, Jr, John T. Brennan, James S. Blank, Latham & Watkins, New York, NY, Michael Chertoff, Latham & Watkins, Newark, NJ, (Charles P. Baker, Robert H. Fischer, Michael P. Sandonato, Fitzpatrick, Cella, Harper & Scinto, New York, NY, of counsel) for Defendants.

OPINION

WOLIN**, District Judge.**

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Before the Court today are two behemoths of the television electronics industry-General Electric Company ("GE") and Nintendo Company, Ltd. ("Nintendo"). FN1 Their respective products, and ones like them, are embedded in the core of the visual society that we have become. Indeed, one would be hard pressed to find someone who does not have a GE product in his home or a person who has never watched a program on a GE television. Likewise, Nintendo products are a lightning rod of interest that electrify the realm of personal entertainment and it is rare to find an individual, at least one of a less-distinguished age than the Court, who has never been challenged by one of the ever-growing number of video games. Ironically, there are probably thousands of homes in which Nintendo video game systems are harmoniously connected to GE televisions. Such harmony is rendered atonal, however, the moment litigation begins.

FN1. Nintendo of America, Inc. is also a named defendant and is, collectively with Nintendo Company, Ltd., referred to as "Nintendo."

GE initiated this action alleging that certain of Nintendo's video game products infringed three separate patents owned by GE. FN2 The patents (and respective claims) under consideration are: United States Patent No. 4,097,899 (Claims 12-14), United States Patent No. 4,169,659 (Claims 1, 3, 4, 5 and 13) and United States Patent No. 4,270,125 (Claim 1). Each of the patents generally relates to electronic circuitry used in connection with television systems. FN3

FN2. Each of the patents at issue here was originally assigned to RCA Corporation ("RCA") and later acquired by GE as part of an asset purchase. *See, e.g.,* Nintendo's '899 Br. at 2 n.3.

FN3. Due to the complexity of the subject matter of the patents, the parties submitted expert certifications with respect to each motion. These certifications were intended, in part, to educate the Court regarding the electronic structure of the patents (and allegedly infringing devices) and the relevance and function of the

patents in the world of television electronics. Each expert certification includes as an exhibit a CD-ROM tutorial discussing the patent and summarizing the opinion of the respective expert. Each CD-ROM runs approximately 45-60 minutes. While generally reiterating the information found in the written expert certifications, the CD-ROMs were of significant use to the Court; as noted, the world in the 1990s is a visual society, of which the Court is a member. The parties and their counsel are to be commended for the high quality of both their written and audio/visual presentations.

Through its present applications for summary judgment, Nintendo seeks a declaration of non-infringement in regard to each of GE's patents. With respect to patent No. 4,097,899, Nintendo alternatively asserts that the patent is invalid by anticipation. FN4 As set out below, the Court has separately analyzed and discussed each of the patents under a single statement of the applicable law. The order of consideration of the patents is random. For the reasons stated herein, the Court will grant Nintendo's motions for summary judgment on each of the three patents.

FN4. Nintendo initially asserted that patent No. 4,270,125 was invalid. In the course of briefing this motion, however, Nintendo withdrew that argument. Nintendo reserved the right to assert invalidity as a defense at trial.

I. LEGAL PRECEPTS

A. Summary Judgment Standard

Rule 56(c) of the Federal Rules of Civil Procedure provides that summary judgment shall be granted if "the pleadings, depositions, answers to interrogatories, and admissions on file, together with the affidavits, if any, show that there is no genuine issue as to any material fact and that the moving party is entitled to a judgment as a matter of law." *See* Hersh v. Allen Prods. Co., 789 F.2d 230, 232 (3d Cir.1986). A dispute involving a material fact is "genuine" only "if the evidence is such that a reasonable jury could return a verdict for the nonmoving party." Anderson v. Liberty Lobby, Inc., 477 U.S. 242, 248, 106 S.Ct. 2505, 2510, 91 L.Ed.2d 202 (1986). The Supreme Court also observed that "[o]nly disputes over facts that might affect the outcome of the suit under governing law will properly preclude an entry of summary judgment." *Id.; see also* Ness v. Marshall, 660 F.2d 517, 519 (3d Cir.1981) (role of district court is to determine whether genuine issue of material fact exists).

Furthermore, when considering a summary judgment motion, this Court must view all evidence submitted in a light most favorable to the party opposing the motion. *See* Matsushita Elec. Indus. Co., Ltd. v. Zenith Radio Corp., 475 U.S. 574, 586, 106 S.Ct. 1348, 1356, 89 L.Ed.2d 538 (1986); Meyer v. Riegel Prods. Corp., 720 F.2d 303, 307 n. 2 (3d Cir.1983), *cert. dismissed,* 465 U.S. 1091, 104 S.Ct. 2144, 79 L.Ed.2d 910 (1984). Although the summary judgment hurdle is a difficult one to meet, it is by no means insurmountable.

Accordingly, in Celotex Corp. v. Catrett, 477 U.S. 317, 106 S.Ct. 2548, 91 L.Ed.2d 265 (1986), the Supreme Court concluded that "[o]ne of the principal purposes of the summary judgment rule is to isolate and dispose of factually unsupported claims or defenses, and we think it should be interpreted in a way that allows it to accomplish this purpose." Id. at 323-24, 106 S.Ct. at 2553.

B. Summary Judgment in Patent Infringement Litigation

[1] The fact that this lawsuit involves a non-infringement analysis or the validity of a patent does not render this case unsuitable for disposition by summary judgment. Although patent infringement cases often raise complex factual issues, "the rules do not change simply because the case involves patent law." Aid Pack, Inc. v. Beecham, Inc., 641 F.Supp. 692, 694 (D.Mass.1986), *aff'd,* 826 F.2d 1071 (Fed.Cir.1987) (citing

D.M.I, Inc. v. Deere & Co., 755 F.2d 1570, 1573 (Fed.Cir.1985)). "Summary Judgment is appropriate in patent cases as in other cases under Rule 56(c)." Procter & Gamble Co. v. Nabisco Brands, Inc., 711 F.Supp. 759, 761 (D.Del.1989).

In fact, the Federal Circuit repeatedly has upheld the grant of summary judgment in patent infringement cases where there was no genuine issue of material fact. *See, e.g.,* George v. Honda Motor Co., Ltd., 802 F.2d 432, 434 (Fed.Cir.1986); Porter v. Farmers Supply Serv., Inc., 790 F.2d 882, 884 (Fed.Cir.1986); Brenner v. United States, 773 F.2d 306, 308 (Fed.Cir.1985); Builders Concrete, Inc. v. Bremerton Concrete Prods. Co., 757 F.2d 255, 257-58 (Fed.Cir.1985); Prodyne Enterprises, Inc. v. Julie Pomerantz, Inc., 743 F.2d 1581, 1583 (Fed.Cir.1984); Molinaro v. Fannon/Courier Corp., 745 F.2d 651, 654 (Fed.Cir.1984).

Thus, the Federal Circuit has advised: "[w]here no issue of material fact is present ... courts should not hesitate to avoid an unnecessary trial by proceeding under Fed.R.Civ.P. 56 without regard to the particular type of suit involved." Chore-Time Equip., Inc. v. Cumberland Corp., 713 F.2d 774, 778-79 (Fed.Cir.1983).

"In accordance with *Chore-Time,* it is incumbent on the trial judge to look beyond mere denials or arguments with respect to issues of scope and content of the prior art, differences between the prior art and the invention in suit, level of skill in the art or other factual issues." Union Carbide Corp. v. American Can Co., 724 F.2d 1567, 1571 (Fed.Cir.1984).

It is with these tenets in mind that the Court considers the defendants' summary judgment motions.

C. Patent Infringement

[2] An infringement analysis requires two separate steps. First, the court must construe the claims asserted to be infringed as a matter of law in order to establish their meaning and scope. *See* Markman v. Westview Instruments, Inc., 517 U.S. 370, 116 S.Ct. 1384, 1393, 134 L.Ed.2d 577 (1996). Second, the claims as construed are then compared to the allegedly infringing device. *See id.* In this latter step, patent infringement may be found in either of two ways: literal infringement or infringement under the doctrine of equivalents.

1. Claim Construction

[3] [4] Since Markman v. Westview Instruments, Inc., 52 F.3d 967 (Fed.Cir.1995), *aff'd,* 517 U.S. 370, 116 S.Ct. 1384, 134 L.Ed.2d 577 (1996), the interpretation of patent claim terms falls within the exclusive province of the Court. The standard to be applied for claim construction is what one of ordinary skill in the art at the time of the invention would have understood the term to mean. *See* id. at 986. The process is akin to statutory interpretation and must be viewed through the lens of objectivity with no inquiry as to the subjective intent of the inventor. *See* id. at 985-87. Thus, to ascertain the meaning of a patent claim a court should examine (1) the claims of the patent, (2) the specification, (3) the patent's prosecution history, and (4) extrinsic evidence. *See* id. at 979-81.

[5] The claims establish the limits or boundaries of the patent while the specification, of which the claims are a part, contains a written description of the invention that would enable one of ordinary skill in the art to make and use the invention. *See* id. at 979-80. "For claim construction purposes, the description may act as a sort of dictionary, which explains the invention and may define terms used in the claims." *Id.* (quoting In re Vogel, 422 F.2d 438, 441 (C.C.P.A.1970)). Indeed, a patentee can be his own lexicographer. *See* id. at 980 (citing Autogiro Co. of Am. v. United States, 181 Ct.Cl. 55, 384 F.2d 391, 396-98 (1967)). The written description, however, "does not delimit the right to exclude. That is the function and purpose of claims." *Id.*

[6] [7] Prosecution history is of primary significance to claim construction; it permits scrutiny of the

proceedings that occurred in the United States Patent and Trademark Office (the "Patent Office"). *See* id. at 980. "The court has broad power to look as a matter of law to the prosecution history of the patent in order to ascertain the true meaning of language used in the patent claims." *Id*. Yet, like the written description, the prosecution history cannot "enlarge, diminish, or vary" claim limitations. *Id*. (citing Goodyear Dental Vulcanite Co. v. Davis, 102 U.S. 222, 227, 26 L.Ed. 149 (1880); Intervet Am., Inc. v. Kee-Vet Labs. Inc., 887 F.2d 1050, 1054 (Fed.Cir.1989)).

[8] Lastly, extrinsic evidence through expert testimony lends understanding to the patent boundaries, but also may not vary or contradict the claims themselves. *See id*. at 980-81. "The court may, in its discretion, receive extrinsic evidence in order 'to aid the court in coming to a correct conclusion' as to the 'true meaning of the language employed' in the patent." *Id*. at 980 (quoting Seymour v. Osborne, 78 U.S. (11 Wall.) 516, 546, 20 L.Ed. 33 (1871)).

Upon consideration of the above, the Court must determine, as a matter of law, the meaning of the claim language at issue.

2. Literal Infringement

[9] Literal infringement occurs whenever a limitation of the patent is literally found in the accused device. *See* SmithKline Diagnostics, Inc. v. Helena Labs. Corp., 859 F.2d 878, 889 (Fed.Cir.1988). To literally infringe, the accused device must contain every limitation of the asserted claim. *See* Laitram Corp. v. Rexnord, Inc., 939 F.2d 1533, 1535 (Fed.Cir.1991).

3. Doctrine of Equivalents

[10] Even if the accused device does not literally infringe, it may still infringe under the doctrine of equivalents "if there is 'equivalence' between the elements of the accused product or process and the claimed elements of the patented invention." Warner-Jenkinson Co., Inc. v. Hilton Davis Chem. Co., --- U.S. ----, ----, 117 S.Ct. 1040, 1045, 137 L.Ed.2d 146 (1997) (citing Graver Tank & Mfg. Co. v. Linde Air Prods. Co., 339 U.S. 605, 609, 70 S.Ct. 854, 856-57, 94 L.Ed. 1097 (1950)). In order for infringement to occur under the doctrine of equivalents, the accused device must perform substantially the same function in substantially the same way to achieve substantially the same overall result as the claimed invention. *See* Graver Tank & Mfg. Co., 339 U.S. at 608, 70 S.Ct. at 856; Pennwalt Corp. v. Durand-Wayland, Inc., 833 F.2d 931, 934 (Fed.Cir.1987), *cert. denied,* 485 U.S. 961, 108 S.Ct. 1226, 99 L.Ed.2d 426 (1988); *see also* International Visual Corp. v. Crown Metal Mfg. Co., Inc., 991 F.2d 768, 773-74 (Fed.Cir.1993) (Lourie, J., concurring) (quoting Graver Tank & Mfg. Co., 339 U.S. at 608, 70 S.Ct. at 856).

[11] Application of the doctrine of equivalents requires evaluating the equivalency of an element or part of the invention with one that is substituted in the accused product. Because each element contained in the patent claim is deemed material, the equivalency analysis must be directed to individual elements of the claim and not to the invention as a whole. As Justice Thomas pointed out in *Warner-Jenkinson,* whether equivalency is expressed in terms of the "triple identity" test focusing on function, way, and result, or is decided through an "insubstantial differences" analysis, is less important than whether the test is probative of the essential inquiry: "Does the accused product or process contain elements identical or equivalent to each claimed element of the patented invention?" 520 U.S. at ----, 117 S.Ct. at 1054. Thus, the determination of equivalence should be applied through an objective inquiry on an element-by-element basis at the time of infringement. *See id*.

[12] [13] Although equivalency under the doctrine of equivalents is a question of fact, it should not be employed to rewrite claims or to rescue the patentee's claim from a determination of non-infringement. Hence, application of the doctrine of equivalents is the exception and not the rule. *See* London v. Carson

Pirie Scott & Co., 946 F.2d 1534, 1538 (Fed.Cir.1991).

D. Invalidity by Anticipation

A product is not patentable unless it is new. Determining whether a product is "new" within the meaning of the patent statute requires comparing the product with the products of the relevant prior art. *See* Shatterproof Glass Corp. v. Libbey-Owens Ford Co., 758 F.2d 613, 619 (Fed.Cir.), *cert. dismissed,* 474 U.S. 976, 106 S.Ct. 340, 88 L.Ed.2d 326 (1985). If a single piece of relevant prior art contains all the elements of the patent at issue, the prior art is said to have anticipated the patent. *See* Structural Rubber Prods. Co. v. Park Rubber Co., 749 F.2d 707, 715-16 (Fed.Cir.1984).

Under 35 U.S.C. s. 102(b), a patent is invalid as anticipated if the claimed invention:

was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of the application for patent in the United States.

Courts have interpreted s. 102(b) to require that "each and every element as set forth in the claim [be] found, either expressly or inherently described, in a single prior art reference." Constant v. Advanced Micro-Devices, Inc., 848 F.2d 1560, 1570 (Fed.Cir.), *cert. denied,* 488 U.S. 892, 109 S.Ct. 228, 102 L.Ed.2d 218 (1988); *see also* Minnesota Mining & Mfg. Co. v. Johnson and Johnson Orthopaedics, Inc., 976 F.2d 1559, 1565 (Fed.Cir.1992).

[14] [15] To determine whether a patent is anticipated by prior art under s. 102(b), the Court must undertake a three-step analysis. The first step is construction of the patent claims to determine their meaning in light of the specification and prosecution history. The second step requires the Court to compare the properly construed claims with the subject matter described in the prior art reference and identify the corresponding elements disclosed in the allegedly anticipating reference. *See* Titanium Metals Corp. of Am. v. Banner, 778 F.2d 775, 782 (Fed.Cir.1985). The third step requires the Court to determine whether the prior art reference is enabling, thereby placing the allegedly disclosed matter in the possession of the public. *See* Akzo N.V. v. United States Int'l Trade Comm'n, 808 F.2d 1471, 1479 (Fed.Cir.1986), *cert. denied,* 482 U.S. 909, 107 S.Ct. 2490, 96 L.Ed.2d 382 (1987). Accordingly, a prior art reference in a printed publication cannot anticipate an invention under s. 102(b) unless it enables one skilled in the art to produce the invention described in the patent.

[16] Defendants must prove anticipation by clear and convincing evidence. *See* Texas Instruments Inc. v. United States Int'l Trade Comm'n, 988 F.2d 1165, 1177 (Fed.Cir.1993) ("A patent is presumed valid and the party asserting invalidity must overcome this presumption by clear and convincing evidence establishing the facts which support the conclusion of invalidity.") (citing Intel Corp. v. United States Int'l Trade Comm'n, 946 F.2d 821, 834 (Fed.Cir.1991)); *see also* Dennison Mfg., Co. v. Panduit Corp., 475 U.S. 809, 810, 106 S.Ct. 1578, 1578-79, 89 L.Ed.2d 817 (1986).

II. UNITED STATES PATENT NO. 4,097,899

A. Background

United States Patent No. 4,097,899 (the " '899 patent"), was issued by the Patent Office on June 27, 1978. It is described as a Video Record Player Switching System. The alleged infringement centers on Claims 12, 13 and 14 of the '899 patent. Claims 13 and 14 are dependent on Claim 12. Claim 12 provides as follows:

12. Video record player apparatus comprising:

a player RF signal input terminal;

a player RF signal output terminal;

a player power supply developing supply potentials when selectively enabled;

means, rendered operative in response to supply potential development by said power supply, for forming a player output signal inclusive of picture carrier frequency oscillations and sound carrier frequency oscillations;

means, responsive to supply potential development by said player power supply, for establishing a first signal path between said output signal forming means and said player RF signal output terminal; said first signal path being disrupted in the absence of supply potential development by said player power supply; and

means, responsive to the absence of supply potential development by said player power supply, for establishing a second signal path between said player RF signal input terminal and said player RF signal output terminal; said second signal path being disrupted in the presence of supply potential development by said player power supply.

Roberge Cert. Ex. A at col. 9, line 62 to col. 10, line 18.

In lay terms, this patent claim discloses a radio frequency switch that directs RF FN5 signals from the video record player to the television receiver and at the same time blocks the flow of broadcast signals from the antenna to the television receiver. When the power to the video record player is off, the signal path from the antenna to the television experiences a low series impedance FN6 and is virtually unaffected; the signal from the antenna freely travels to the television. When the power to the video record player is on, the signal path from the antenna to the television receiver is disrupted by a high series impedance-an open electro-mechanical relay. FN7 Concurrent to the disrupt function is a bypass function, which diverts a substantial portion of the antenna television signal to ground. The bypass function is accomplished through the use of an energized diode. FN8 Hence, the '899 patent claims both a disrupt function and a bypass function, the former performed by an electro-mechanical relay, and the latter achieved through the use of an energized diode.

FN5. An RF signal is a signal in the radio frequency range.

FN6. In simplified terms, "impedance" can be understood as a measure of the degree of difficulty of passing current through a two terminal electric component. The higher the impedance of the component, the more difficult it is to pass current through that component.

FN7. An electro-mechanical relay acts like a signal bridge and reacts to a power supply. An open relay serves as a high series impedance because of the resulting physical gap in the signal path.

FN8. As used here, a diode is an electronic switch that is normally non-conductive to RF signals, or "off," but when a certain current flows through it, the diode becomes conductive to RF signals, or "on."

1. Function and Structure of the '899 Patent

The '899 patent is a means plus function patent. At column 10, lines 4-10, the video record player signal

path is designated as the first signal path, and at lines 11-17, the signal path between the antenna and the television receiver is referred to as the second signal path. *See* Roberge Cert. Ex. A at col. 10 lines 4-10 and 11-17.

When the video player's power supply is on, each of the signal paths is affected simultaneously. First, the second signal path from the antenna to the television is disrupted through a high series impedance caused by the opening of the electro-mechanical relay, designated as relay (50) in the patent. *See* id. Ex. A, Fig. 1 ("App. 1").FN9 At the same time in the second signal path, diode (66) is energized and rendered conductive to permit a substantial portion of the antenna signal to be bypassed away from the antenna/television receiver signal path and sent to ground. *See* id. In the first signal path, video player RF signals, generated by transmitter (30), are sent through conductive diode (62) to the television receiver. Thus, when the video player power is on, the television receives only a signal from the video player, and the broadcast RF signals from the antenna are prevented from being transmitted to the television receiver. Also, because relay (50) is open, the video player RF signals are prevented from being transmitted to the antenna.

FN9. A diagram of the '899 patent is attached hereto as Appendix 1.

When the video player switch is in the off position, no RF signal is transmitted, diodes (62) and (66) are non-conductive, and relay (50) is closed. By this process, broadcast signals are transmitted from the antenna to the television receiver without disruption (nor are they bypassed to ground), while the first signal path between the video player and the television receiver is disrupted.

2. Nintendo's Denial of Infringement and Claim of Invalidity

Nintendo denies that its Nintendo Entertainment System ("NES") and Super Nintendo Entertainment System ("SNES") are covered by Claims 12-14 of the '899 patent. It asserts that these Nintendo systems employ an RF switch that is covered by Nintendo's U.S. Patent No. 4,745,478 (the " '478 patent") which is entitled "RF Switch" and was issued by the Patent Office on May 17, 1988. The '899 patent was not a cited reference in the '478 patent.

At the very outset, Nintendo contends that its switch does not contain a disrupt function and therefore cannot infringe the '899 patent literally or through the doctrine of equivalents. Moreover, Nintendo insists, the structure of its bypass function with respect to the antenna/television receiver path is significantly different. Apart from function and structure, Nintendo argues that its NES and SNES systems are not video record players and fall outside the claims of the '899 patent.

a. Nintendo's RF Switch

The RF switch used by Nintendo in its NES and SNES video game systems is the RF switch described in the '478 patent. Not unlike the '899 patent, the purpose of the RF switch in the '478 patent is to inhibit the antenna input of a television receiver when the television receiver is used as a monitor for a picture processing system, such as a personal computer, a video game system, or the like. *See* Roberge Cert. Ex. G, col. 1, lines 7-12; col. 1, lines 29-44. While the '899 patent speaks of first and second signal paths, the '478 patent describes the signal as a first television signal and a second television signal.FN10

FN10. In the '478 patent (and elsewhere in the documents relevant to this litigation), "TV" is often used to refer to television.

The Nintendo RF switch employs a system that primarily utilizes three-stage high-pass filters and three

switching transistors. *See* id. Ex. G, Fig. 2 ("App. 2") (denoting three-stage high-pass filters as 50a, 50b and 50c and three switching transistors as 52a, 52b and 52c).FN11 When the television receiver is used as a television receiver and not as a monitor, the first television signal from the television antenna is transmitted through the active three-stage filters to the television receiver. Under this scenario, the switching transistors remain off and the respective filters are not disabled. This electronic architecture permits the television signal from the television antenna to go to the receiver without interference.

FN11. A diagram of the '478 patent is attached hereto as Appendix 2.

Conversely, when the power switch to a game apparatus is turned on, the second television signal, also termed the "TV game signal," is applied to the television receiver which is used as a monitor. When this occurs, the first television signal is grounded and thereby automatically disabled. This happens because switching transistors 52a-52c are turned on and high-pass filters 50a-50c are disabled. Nintendo describes this as a "bypass" function with respect to the antenna/television path. Nintendo's Br. at 9.

Because Nintendo's RF switch does not place any disrupting component, such as an electro-mechanical relay, in the signal path between the antenna and the television receiver, Nintendo contends that the disrupt function of the '899 patent is lacking.

b. Nintendo's Arguments in Support of the Lack of Equivalency Between the Function and Structure of the '899 Patent **as Compared to** the '478 Patent

Distinct from its lack of disruption non-infringement argument, Nintendo contends that Claim 12 of the '899 patent is a video record player apparatus containing an RF switch. Therefore, because of the "video record player" claim limitation, Nintendo reasons that its NES and SNES, characterized as video game systems, are not covered. Nintendo bottoms its argument by pointed references contained in the '899 patent. In column 1, lines 9-10, the video record player is described as an "apparatus for playback of a recording of picture representative video signals." Roberge Cert. Ex. A. An illustrative example of such a player system is a "video disc player" found at column 1, lines 15-16. Id. Moreover, Nintendo's expert, James K. Roberge, through his certification informs that a video disc player is completely passive in its operation; it does not generate any information itself and it does not alter the information contained in any of the signals it receives. *See* id. para. 43. Rather, it simply converts those signals to a format compatible with a television monitor. *See* id.

Noteworthy in Nintendo's analysis is the functional dissimilarity between Nintendo's video game systems and the video record player referenced in the '899 patent. Nintendo characterizes its systems as an "interactive" system, as opposed to a passive system, that solely retrieves stored information. By use of the term "interactive," Nintendo describes a system where the user is provided real time control over the images that are created. *See* id.

Another consideration advanced by Nintendo to contrast the '899 RF switch and the '478 RF switch is the latter's portability. Because Nintendo's RF switch can be moved away from the television and located with the user, it is free of the constraints that are inherent to the '899 RF switch, which is designed to be internal to the video record player. The '899 switch was designed for use with a stationary device that would sit atop or adjacent to the television monitor. Indeed, the inventor of the '899 RF switch, John Yu, never considered the portability of the switch or locating the switch outside the video record player. *See* Mascaro Cert. Ex. 3 at 29-30 and 60-65.

c. Nintendo's Invalidity Claim: Anticipation of the '899 Patent

Nintendo's invalidity claim is grounded on the theory that the '899 patent was anticipated by a Japanese patent application published more than one year prior to the filing date of the '899 patent application. More particularly, Nintendo asserts that a prior art reference filed with the Japanese Patent Office on behalf of Sharp Corporation, Patent Application SHO 49-7211 ("Sharp II") disclosed a switching operation that would have enabled one skilled in the art to produce the RF switch disclosed in the '899 patent.FN12 Because the claimed invention described in Sharp II preceded the '899 patent and was published more than one year in advance of the '899 patent's date of application for patent in the United States, Nintendo asserts that Sharp II anticipated, and therefore invalidates, the '899 patent.

FN12. Nintendo asserts that the '899 patent was anticipated by both Sharp II and a preceding Japanese patent application, No. 50-16919 ("Sharp I"). *See* Roberge Cert. para.para. 12-13, 44. Nintendo believes that both Sharp I and Sharp II disclose each of the elements of the '899 patent. Nintendo, however, has relied primarily on Sharp II as the invalidating prior art reference. *See* id. para. 46; Nintendo's Br. at 34-37. As such, the Court will focus its prior art discussion herein on Sharp II.

3. GE's Reply to Nintendo's Non-Infringement and Claim Construction Analysis

GE alleges both literal infringement and infringement through the doctrine of equivalents. Central to GE's argument is the premise that the '899 patent is a novel combination of RF switch and RF modulation. GE reasons that, under the '899 patent, when the power supply to the video record player is on, a "quieting feature" silences the television receiver's sound channel and turns the screen into a solid color. Conversely, when the video record player power supply is off, the television receives the broadcast RF signals directly from the antenna, a function which serves to improve the television receiver's broadcast picture quality. GE further asserts that the disruption and bypass function of the '899 patent also solves the problem of signal leakage and eliminates interference with broadcast signals received by neighboring antennae. Lastly, GE disputes the narrow claim construction proffered by Nintendo that its NES and SNES entertainment systems are not video record players.

GE argues that the NES and SNES video game systems are, in fact, video record players. It disavows that use of the phrase "video record player," as set forth in the preamble to Claim 12, is a term of limitation. Similar to Nintendo, GE points to references in the patent description that it terms as the environment for the invention. GE maintains that the phrases "other video information services" found at column 1, lines 6-7, and "playback apparatus" used at column 2, line 30, are examples that demonstrate the breadth of the claim beyond a video record player. Lastly, GE portrays the NES and SNES systems as an apparatus for playback of a recording of picture representative signals. It avers that video and audio signals begin playing in a prearranged format as soon as the power to the NES or SNES system is turned on, not unlike the function of the '899 video record player. The Nintendo system is therefore passive, and becomes interactive only when the game controls are used; when the game controls are inactive, one could sit and watch the screen play prerecorded, changing scenes and pictures, including moving characters and background. *See* GE's Br. in Opp. at 28.

4. Expert Testimony

a. Kurt Wallace for GE

Kurt Wallace ("Wallace") styles himself as a practicing engineer in the field of television-related electronics for more than thirty-five years. *See* Wallace Decl. para. 1. During this period of practice he has designed, developed and researched video recording and broadcast television equipment. *See* id. para. 2. After an examination of the '899 patent and its file history, the NES and SNES systems, and the '478 patent, Wallace concludes that the two Nintendo systems incorporate each of the elements of Claims 12, 13 and 14 of the '899 patent. *See* id. para. 4. Moreover, he concludes that neither the Sharp I nor the Sharp II patent

applications anticipated the '899 patent. *See* id. para. 5.

The first thirty paragraphs of the Wallace declaration explain the operation of the switching circuit disclosed in the '899 patent. This operation is defined in terms of impedance to ground, a relative concept whose application depends upon the presence or absence of a developed power supply voltage. In paragraph 31, Wallace summarizes the invention as follows:

When power supply voltage is not developed, the impedance between an antenna and the TV is low relative to the impedance to ground. Hence, the broadcast RF signals from the antenna are transmitted to the TV rather than to ground. When power supply voltage is developed, the impedance between the player and the TV is low relative to the impedance to ground. Also, the impedance between the antenna and television is high relative to the impedance to ground. As a result, the RF signals from the player are transmitted to the TV and the broadcast RF signals from the antenna are passed to ground.

See id. para. 31.

For purposes of the infringement analysis, Wallace examined the NES system's circuitry and observed its operation. He concludes that the NES system is a video record player because the RF modulator unit creates an RF output signal that is transmitted to the RF switch and permits the video and audio data to be converted into television signals from the player to be played on a television monitor. *See* id. para. 34. Wallace further concludes that the NES system incorporates an RF signal input and output terminal as claimed in elements (1) and (2) of the '899 patent. *See* id. para. 35. Wallace also concludes that the NES system incorporates a player power supply that is selectively enabled, as claimed in element (3) of the '899 patent. *See* id. para. 36.

The fourth element of the '899 patent provides for a "means, rendered operative in response to supply potential development by said power supply, for forming a player output signal inclusive of picture carrier frequency oscillations and sound carrier frequency oscillations." *See* Roberge Cert. Ex. A, col. 9, line 67 to col. 10, line 3. A comparison of the NES system and the circuitry described in the '899 patent is accomplished by Wallace in paragraph 41 of his declaration. By an examination of oscillation circuits, Wallace determines that the NES system incorporates the circuitry that forms an RF output signal to quiet the television, as claimed in element (4) of the '899 patent. *See* Wallace Decl. para. 41.

Elements (5) and (6) of the '899 patent establish first and second signal paths. The presence of either of these signal paths depends upon whether power to the video record player is on or off. Because Wallace determines that the NES system is a video record player, he finds that the NES system circuitry likewise includes two signal paths: "One signal path between the antenna and the TV is established whenever power to the NES player is absent. The other signal path between the player and the TV is established whenever power is applied to the NES player." *See* id. para. 42. Wallace describes the circuitry operation as follows:

The signal path between the NES player and the TV (the "first signal path" of claim 12) is established when power is applied to the NES as in the circuitry of the '899 patent. Also, when the signal path between the NES player and the TV is established, the signal path between the antenna and the TV (the "second signal path" of claim 12) is disrupted just like in the circuitry of the '899 patent. Disrupting the path between the antenna and the TV requires that television signals from the NES player are prevented from passing to the antenna and broadcast RF television signals from the antenna are prevented from passing to the TV. Further, when the power is not applied to the NES player, broadcast RF television signals pass to the TV but are prevented from passing to the NES player along the path between the NES player and the TV as in the circuitry of the '899 patent. Thus, the NES includes circuitry for establishing first and second paths in response to the development, or absence of, the power supply.

See id. para. 43.

Paragraph 46 of the Wallace affidavit is critical to the equivalency necessary for GE to sustain its '899 patent infringement argument against Nintendo. In that paragraph, Wallace confirms that when a power supply voltage is developed, the first signal path, the path between the NES player and the television, is established. At this time, Wallace asserts, the NES switching circuitry disrupts the second signal path, the path between the antenna and the television. Wallace concludesthat the NES switching circuitry effectively bars RF signals from passing from the NES player to the antenna and also effectively bars broadcast television signals received at the antenna from passing to the television. *See* id. para. 46. This "effective bar" is illustrated in paragraphs 47 and 48 of his declaration and occurs as the result of the implementation of a combination of capacitors, resistors and transistors, whose interplay is defined in terms of high and low impedance. *See* id. para.para. 47-48.

In paragraphs 52-54, Wallace provides his analysis of the structure and interchangeableness of the switching circuitry found in both the NES system and the '899 patent. Because of the interconnected operation of the components of the NES system and the '899 patent, and the similarity that exists between them, Wallace reasons that a person of ordinary skill in the field of television-related electronics would find the circuitry of the NES RF switch to be functionally interchangeable with the switch circuitry of the '899 patent. Thus, he concludes, the NES system incorporates the circuitry of elements (5) and (6) of Claim 12 of the '899 patent. *See* id. para. 54.

Moreover, Wallace finds that the dependent claims of the '899 patent, Claims 13 and 14, are likewise present within the NES. *See* id. para.para. 55-56.

While Wallace devotes much of his declaration to an evaluation of the NES system and its circuitry, paragraphs 58 through 63 detail why he thinks all the elements of Claims 12, 13 and 14 of the '899 patent are also incorporated in the SNES system. Wallace indicates that he has observed the SNES system and has reviewed Katsuya Nakagawa's ("Nakagawa") certification.FN13 *See* id. para. 57. Following this review, Wallace avers that the RF switch in the SNES system is comprised of the same circuitry as the RF switch in the NES system and operates in the same fashion.

FN13. Nakagawa supervised the design of the RF switch used with both the NES and SNES systems. Nintendo included Nakagawa's certification as part of its written submissions.

b. James Roberge for Nintendo

James Roberge ("Roberge") is a professor of electrical engineering at the Massachusetts Institute of Technology. He teaches and conducts research in the field of electronic circuits and their design. *See* Roberge Cert. para. 1. He has specific experience in the design of electronic circuits using frequencies in the RF range. *See* id. para. 2.

Professor Roberge studied the '899 patent, the '478 patent, Nakagawa's certification, and the deposition transcript and exhibits of John Yu ("Yu"), the named inventor of the '899 patent. *See* id. para. 4. At paragraph 5 of his certification, Professor Roberge concludes that Nintendo's NES and SNES systems do not infringe Claims 12-14 of the '899 patent. His conclusion of non-infringement is threefold:

1. The RF switch used in the NES and SNES does not perform the claimed function of disrupting the second signal path.

2. The structure described in the '899 patent for performing the claimed functions is not the same or

equivalent to the structure used in the Nintendo RF switch.

3. The NES and SNES are not "video record players" as required by claims 12 to 14 of the '899 patent.

See id. para. 5.

From paragraph 15 through paragraph 25 of his certification, Professor Roberge explains the function of the '899 patent when the video record player is in both the on and off position. Thereafter, in paragraphs 26 and 27, he explains the manner in which the Nintendo RF switch operates. Critical to its operation are three transistors,FN14 which are connected between the antenna-television signal path and ground. When the power to the NES or SNES is off, the three transistors are off; when the Nintendo systems are turned on, the transistors are likewise turned on. In the "on" position, the transistors provide three low impedance shunts to ground. Because the impedance of these shunts is low, Professor Roberge reasons that it is far easier for the antenna signal to travel down those additional paths to ground than to travel to the television receiver. *See* id. para. 26. Roberge states that, unlike the '899 patent, the Nintendo RF switch does not contain any component that creates a high series impedance, such as an electro-mechanical relay in the antenna to television signal path. *See* id. para. 27. With the Nintendo RF switch, a direct path always exists between the antenna and the television receiver.FN15

FN14. These transistors are used as electronic switches. They allow signals to flow when they are on and do not allow signals to flow when they are off.

FN15. The direct path is through three fixed value capacitors found in three high-pass filters. A capacitor is an electronic component that is conductive to RF signals but not conductive to DC signals. A fixed value capacitor is not a switching component. *See* Roberge Cert. para. 27 and n. 8.

Support for Professor Roberge's analysis that the Nintendo RF switch does not disrupt the signal path like the '899 patent, but instead redirects the signal (the bypass function) to ground, is contained in paragraphs 29 through 33 of his certification. In those paragraphs, Roberge explains that to disrupt a signal path by introducing a high series impedance is to break the path. On the other hand, to bypass a signal is to redirect that signal along an alternative path to another point. Hence, he concludes that in the realm of RF circuit art, disrupt and bypass are separate functions. When a signal path is broken, current flow stops. When a signal path is bypassed, the current flows away from the signal path but is not stopped. Because of this fundamental difference in RF circuit art, Roberge concludes, Nintendo's three transistors operate in a substantially different way from the electro-mechanical relay embodied in the '899 patent. *See* id. para. 32.

Moreover, Roberge asserts, the structure of the corresponding RF switches is significantly different. Nintendo's RF switch, as described in the '478 patent, is a purely electronic switch. In contrast, the electro-mechanical relay of the '899 patent relies on mechanical means to disrupt the signal path. Again Roberge avers that in the art of RF circuit design, a relay directly in the path that disrupts the path would not be considered equivalent to the Nintendo combination of switching components; the switching components are not placed directly in the antenna-television path, and they only bypass that signal path to ground. *See* id. para. 36.

In paragraph 43 of his certification, Professor Roberge distinguishes from a technical standpoint the difference between video record players and video game systems. He concludes that they are substantially different devices. Video record players contain electronic circuitry that allows them to play back pre-recorded signals for viewing on a television set. Video game systems, like the NES and SNES systems, contain picture processing units, other specialized chips, and digital logic circuitry that execute a game

program stored in a cartridge. When the video game system is activated, interactive images are generated on a television set as the user manipulates the controls of the game. If a user, for example, were to shoot an object displayed on the screen, the image on the screen would change. *See* id. para. 43.

c. Katsuya Nakagawa for Nintendo

Nakagawa is one of the listed inventors of the RF switch which is described in the '478 patent. *See* Roberge Cert. Ex. G (copy of Patent Number 4,745,478 issued May 17, 1988). The '899 patent is not a cited reference for the '478 patent. By his certification, Nakagawa informs that he supervised the design of the RF switch used with both the NES and SNES home video game systems. *See* Nakagawa Cert. para. 1. This design was an RF switch which would be used to switch between the broadcast television signal received through the antenna and the video game system RF signals. *See* id. para. 2. Nakagawa acknowledges that the SNES system, Nintendo's second generation home video game system, uses the same RF switch as used in the NES system. *See* id. para. 3.

In paragraph 5 of his certification, Nakagawa voices his familiarity with the various RF switches that were already on the market when he began work on the Nintendo RF switch. Video tape recorders, for example, utilized an RF switch that was located inside the video tape recorder console. Video game RF switches, although located outside of the video game console, were still connected betweenthe console and the receiver and typically had to be operated manually. *See* id. para. 5.

Nakagawa wanted to design an RF switch that would be a separate device and that would be located outside of the video game console. *See* id. para. 6. By this design, he envisioned that players of the system, especially children, could move the video game console during use. Video tape recorders lack this flexibility of movement because the RF switch is located inside the video tape recorder console. *See* id. Moreover, with an external RF switch, the video game console can be readily disconnected without breaking the connection between the antenna and the television. Thus, a player may disconnect the console from one television set and connect it to another. *See* id. para. 7.

Another feature of the Nintendo RF switch specifically desired by Nakagawa was its automatic nature; Nakagawa sought to design the Nintendo RF switch to switch from the antenna to the video game whenever power for the video game was turned on. Conversely, when the power for the video game was turned off, Nakagawa wanted the RF switch to switch to the antenna. *See* id. para. 8. To accomplish this, Nakagawa designed the RF switch with all electronic components. He rejected the electro-mechanical relay approach because it was more expensive, required more power, and was less reliable than an electronic switch. *See* id. para. 10.

In paragraph 13 of his certification, Nakagawa catalogues his specifications for the Nintendo RF switch. They may be summarized as follows:

-> The RF switch should be external and remote from the video game console.

-> The RF switch should have the power and RF signals superimposed on a single wire.

-> The RF switch should be all electronic.

-> The RF switch should provide isolation when the video game is on.

-> The RF switch should pass the signal received by the antenna to the television with very little weakening of that signal when the video game is off.

-> The RF switch should not require power in order to operate when the video game is off.

-> The RF switch should have a low cost.

Id. para. 13.

The RF switch for the NES system uses a combination of high pass filters in the signal path between the antenna and the television. Nakagawa describes its operation as follows:

[W]hen the video game is off, the filters permit broadcast signals from the antenna to travel to the television receiver with very little signal loss. Three active switching components called transistors within the high pass filters are connected between the signal path and ground. When the video game is turned on the power is supplied to its three transistors, each of which creates a bypass between the signal path and ground. This shifts the cutoff frequency of the high pass filters to frequencies higher than channels 3 and 4 (the channels on which the video game is designed to operate), and an isolation of 65 decibels or higher is provided between the antenna and the television receiver at channels 3 and 4 when the video game is on.

Id. para. 15.

Additionally, Nakagawa rejected components that would actively provide isolation in the signal path between the antenna and the television receiver. *See* id. para. 16. He characterizes these type of components as unacceptable because they would have blocked or significantly weakened the signal received by the antenna when power to the video game was off. Instead, he opted for and used transistors as active components between the antenna television path and ground. By implementation of these transistors, he created isolation by changing the characteristics of the filters table by redirecting or bypassing the RF signal to ground. *See* id.

Nakagawa viewed his design as novel and was unaware of the RF switch disclosed in the '899 patent when he conceived, and subsequently patented, the '478 switch. *See* id. para.para. 17-18. After he read the '899 patent, Nakagawa concluded that the teaching of the relevant claims of the '899 patent would not have provided any assistance to him. In support of this statement, he sets forth three reasons, as follows:

1. In order to lower cost and achieve better reliability, I decided that the Nintendo RF switch should be designed to use all electronic components. In contrast, the '899 patent discloses an RF switch which uses an electromechanical relay switch. In general, electromechanical relays are more expensive and less reliable than electronic components.

2. I designed the Nintendo RF switch so that it has no electronic switching components in the signal path. Instead, three transistors redirect the signal to ground causing signals of the appropriate frequency to be by-passed, or redirected to ground. In contrast, the system disclosed in the '899 patent contains an electromechanical relay switch in the path between the antenna and the television set.

3. Because I wanted the Nintendo RF switch to be external and because I did not want to have a separate power line to the RF switch, I decided that Nintendo's switch should have both power and the RF signal superimposed on the same line. In contrast, the '899 patent describes an RF circuit which has separate lines for power and for the RF signal.

Id. para. 18.

In the closing paragraph of his certification, Nakagawa opines that "the '899 patent represents a fundamentally different RF switch design that functions in a substantially different way than the Nintendo

RF switch." Id. para. 19.

B. Discussion

1. Non-infringement of Claim 12 of the '899 Patent

Nintendo contends that its NES and SNES systems neither literally infringe the '899 patent nor infringe the '899 patent pursuant to the doctrine of equivalents.

a. Literal Infringement

To literally infringe independent Claim 12 of the '899 patent, every limitation of that claim must be found in Nintendo's accused devices. Claim 12 of the '899 patent is written in "means-plus-function" format. Such a format is provided by statute:

An element in a claim for a combination may be expressed as a means or step for performing a specified function without the recital of structure, material, or acts in support thereof, and *such claim shall be construed to cover the corresponding structure,* material, or acts *described in the specification and equivalents thereof.*

35 U.S.C. s. 112(6) (1984) (emphasis added).

At issue in this patent litigation is the last means-plus-function limitation of Claim 12. That limitation provides "means, responsive to the absence of supply potential development by said player power supply, for establishing a second signal path between said player RF signal input terminal and said player RF signal output terminal; said second signal path being disrupted in the presence of supply potential development by said player power supply." Roberge Cert. Ex. A at col. 10, lines 11-18.

The claimed function of "disrupting" the "second" signal path between the antenna and the television is provided for in the specification. *See id.* Ex. A at col. 1, lines 38-43; col. 4, lines 1-10. When the patentee acts as his own lexicographer, the specification of which the claims are a part may act as a sort of dictionary, which explain the invention and may define terms used in the claims. *See* Markman, 52 F.3d at 979-80. The '899 patent teaches that a signal path is "disrupted" by providing a high series impedance in that path. The second signal path, the path between the antenna and the television, is disrupted by the opening of an electro-mechanical relay. *See* App. 1 at relay (50). The "disrupting function" is separate and distinct from the bypass function performed by diode (66). *See* id. at diode (66).

The RF switch in the NES and SNES systems is a totally electronic switch. It employs a system that relies on the implementation of three-stage high-pass filters and three switching transistors. *See* App. 2 at filters 50a, 50b, and 50c and switching transistors 52a, 52b and 52c. When the television receiver is used as a receiver and not as a monitor, the three-stage filters are activated and permit the television signal to be transmitted from the antenna to the television receiver. At this time, the switching transistors remain off and the filters are not disabled. When the power switch to a NES or SNES system is activated, the switching transistors are energized, and the high-pass filters are disabled. Through this means, the television broadcast signal is bypassed to ground and automatically disabled.

[17] Because the '899 patent disrupts the broadcast television signal in the second signal path by means of an electro-mechanical relay and the Nintendo RF switch contains no switching components that disrupt the signal, the Nintendo RF switch cannot literally infringe the sixth element of Claim 12. *See* Roberge Cert. Ex. A at col. 10, lines 16-18 ("said second signal path being disrupted in the presence of ... power supply"). Nintendo's use of three transistors to redirect the signal to ground causes signals of the appropriate frequency to be bypassed. Consequently, Nintendo's electronic switching circuitry is not the same as or

equivalent to the electro-mechanical switching structure disclosed in the '899 patent.

The meaning and scope of the claims are clear and distinguishable. On comparison, the accused switch employed by Nintendo does not contain every limitation of the asserted claim. Without the presence of the disruption limitation as expressed in the sixth element of Claim 12, no literal infringement has occurred.

b. Infringement Under the Doctrine of Equivalents

Beyond the reasons asserted to counter the allegation of literal infringement, Nintendo also contends that there has been no infringement under the doctrine of equivalents. Nintendo cites the disruption function of the '899 patent as a substantial difference between its RF switch and that of the '899 patent. Additionally, Nintendo asserts that the structure used to accomplish its RF switching is fundamentally different from the structure disclosed in the '899 patent-the Nintendo RF switch only bypasses; it does not conjointly disrupt and bypass.

[18] GE urges that under a function-way-result analysis, the performance of the Nintendo RF switch is the same as the patented device. *See* GE's Br. in Opp. at 29. GE is wrong.

Here, the critical inquiry is whether the accused product, the RF switch in the NES and SNES systems, contains elements identical or equivalent to each claimed element of the patented invention. Through an objective comparison conducted on an element-by-element basis at the time of infringement, the answer is resolutely one of non-infringement. Neither the function nor the structure of the '478 RF switch is identical or equivalent to the function and the structure of the '899 RF switch.

The '478 RF switch is an all-electronic switch that does not disrupt the television broadcast signal when the television receiver is used solely as a monitor. Through switching transistors, when energized, the television broadcast signal is bypassed to ground and automatically disabled. The '899 RF switch, when confronted with the same set of conditions, disrupts the television broadcast signal through the use of an electro-mechanical relay that creates a high level of impedance in the signal path between the antenna and television receiver. Additionally, a substantial portion of the antenna signal is bypassed to ground through diode (66). *See* App. 1 at diode (66). On an objective basis, a one-step electronic process that simply bypasses a signal is neither identical nor equivalent to a two-step process, employing an electro-mechanical device, that both bypasses and disrupts the signal.

GE argues through its expert, Wallace, that the switching circuitry found in both the NES and SNES systems are functionally interchangeable with that of the '899 patent. Wallace reasons that a person of ordinary skill in the field of television related electronics would deem Nintendo's capacitors equivalent to GE's electro-mechanical relay. Yet, capacitors are not switching components and are incapable of the disrupt function performedby the electro-mechanical relay. Instead, the switching function in the '478 patent results solely from bypassing the signal, which occurs when a lower impedance bypass to ground is introduced by a power supply to the video game system. With capacitors, a direct path always exists between the antenna and the television receiver; unlike the '899 circuitry, the direct path between the antenna and the television in the '478 circuitry does not include a high impedance switching device, such as an electro-mechanical relay, which actually disrupts the signal. The capacitors in the Nintendo switch only serve to block DC voltage and do not alter the impedance level, regardless of whether the power supply to the video game is turned on or off. Even Wallace, GE's own expert, admits that capacitors only transmit RF signals. *See* Wallace Decl. para. 19. With respect to the direct path between the antenna and the television, the capacitors in the '478 patent are not equivalent to the electro-mechanical relay in the '899 patent.

The most telling evidence of the lack of equivalence or interchangeableness between the structures of the '478 RF switch and the '899 RF switch is the testimony of the '899 patent's inventor, Yu. Yu's testimony is

recited in Nintendo's memorandum in support of summary judgment at pages 12-13. In its pertinent part, it reads as follows:

During the development of the RF switch structure disclosed in the '899 patent, the named inventor, John Yu, initially designed a structure that included four electro-mechanical relays. Patent Disclosure Form at GE 000101; Yu Tr. at 102 (*see* Mas. Cert., Exs. 2 and 3). Over a period of several months, Mr. Yu continued to work on the design of his RF switch in order to eliminate as many of the electro-mechanical relays as possible. Yu Notebook at GE 003111-12, 003121-22; Yu Tr. at 117, 119-121 (*see* Mas. Cert., Exs. 4 and 3). He did this because he recognized that electro-mechanical relays were not as reliable as electronic switching components. Yu Tr. at 116-117, 119-120 (*see* Mas. Cert., Ex. 3). [footnote 10: In fact, in another part of the device that Yu was working on, he decided to replace an electro-mechanical relay with an electronic switch specifically in order to "increase reliability and to reduce the cost." Yu Notebook at GE 003129 (*See* Mas. Cert., Ex. 4).]

Ultimately, Mr. Yu tried to design an RF switch structure which was all-electronic and included no electro-mechanical relays. However, he was unable to do so. Yu Tr. at 163-165 (*see* Mas. Cert., Ex. 3). When Mr. Yu placed an electronic switching component directly in the antenna/television signal path in order to be able to disrupt that path, it caused an unacceptable loss of antenna signal strength when the power was 'off.' Yu Notebook at GE 003121; Yu Tr. at 144-45, 163-165 (*see* Mas. Cert., Exs. 4 and 3). As a result, Mr. Yu ultimately settled on an RF switch structure which used one electro-mechanical relay in the antenna/television signal path that physically opened and closed the path, and disclosed this structure as the only embodiment in the '899 patent. Yu Memorandum at GE000099; '899 patent, Figure 1 (*see* Mas. Cert., Ex. 5; Rob. Cert., Ex. A). He never designed an acceptable switch that performed its switching function by only bypassing the antenna/television path when the VTR was turned on. Yu Tr. at 138-39 (*See* Mas. Cert., Ex. 3); Rob. Cert. para. 33.

Nintendo's Br. at 12-13.

Logic compels the decision that these RF switches are not structurally identical or equivalent. Certainly, if Yu was unable to design an all-electronic switch sufficiently appropriate to perform the disrupt function, it necessarily follows that a person of ordinary skill in the field of television-related electronics would likewise be unsuccessful.

Beyond the missing disruption function and Nintendo's all-electronic RF switch, other differences counsel against a finding of equivalence between the two devices.

The RF switch disclosed in the '899 patent is a switching system to be used in a video record player. Despite a fervent attempt to categorize the NES and SNES systems as video record players, such effort is unavailing to GE. These Nintendo systems are not merely an "apparatus for playback of a recording of picture representative video signals"as discussed in the '899 patent. Roberge Cert. Ex. A at col. 1, lines 9-10. These video games are interactive and each scene is generated in real-time in response to input from the game player. They do more than simply play back a pre-recorded series of video signals. The video record player, in contrast, is passive in nature, and the specification does not contemplate that the '899 RF switch would have any application in any other system or environment. *See* Nintendo's Br. at 26.

Although GE points to language contained in the specification to demonstrate that the scope of the invention exceeds video record player systems and includes "other video information sources," *see* Roberge Cert. Ex. A, col. 1, line 4, such a vague reference is not sufficient to ensnare systems that were not within the contemplation of the inventor. By contrast, Nakagawa in the '478 patent enumerates picture processing systems such as a personal computer, a video game, or the like. *See* Roberge Cert. Ex. G at col. 1, lines 10-12. Because the '899 RF switch was designed for video record players, the claims at issue should be limited

to that device and not expanded through vague and uninformative language. This is especially true in a crowded art field. As stated in Exxon Chemical Patents, Inc. v. Lubrizol Corp., 64 F.3d 1553, 1563 (Fed.Cir.1995) (Plager, Jr., concurring), *cert. denied,* 518 U.S. 1020, 116 S.Ct. 2554, 135 L.Ed.2d 1073 (1996):

[W]e are not free to read the claims as they might have been drafted, even if as drafted they do not accomplish what the inventor may have intended.

Claim drafting is itself an art, an art on which the entire patent system today depends. The language through which claims are expressed is not a nose of wax to be pushed and shoved into a form that pleases and that produces a particular result a court may desire. The public generally, and in particular, the patentee's competitors, are entitled to clear and specific notice of what the inventor claims as his invention. That is not an easy assignment for those who draft claims, but the law requires it, and our duty demands that we enforce the requirement. There is no room in patent claim interpretation for the equivalent of the *cy pres* doctrine; that would leave the claiming process too indefinite to serve the purposes which lie at the heart of the patent system.

Other differences between the switches demonstrate the lack of identity or equivalence between them. For example, Nakagawa, the inventor of the '478 switch, implemented a design concept that permitted the RF switch to be located outside of the video game console. Unlike RF switches that are located inside a video tape recorder, Nakagawa's RF switch provides portability during use. Moreover, with an external RF switch, the video game console can be readily disconnected without breaking the connection between the antenna and the television. Therefore, a player may disconnect the console from one television set and connect it to another. The '899 RF switch does not permit the choice and convenience of movement. *See* Nakagawa Cert. para. 7.

Seemingly insignificant, but of structural importance, was Nakagawa's decision to eliminate a separate power line to the '478 RF switch. In contrast to the '899 patent, which describes an RF circuit with separate lines for power and for the RF signal, Nakagawa decided that Nintendo's switch should have both power and the RF signal superimposed in the same line. His '478 patent accomplished that goal.

To return to where the analysis began, the Court concludes that there is no infringement under the doctrine of equivalents and Nintendo's summary judgment of non-infringement as to Claim 12 must be granted.

2. Non-infringement of Claims 13 and 14 of the '899 Patent

Because the Court has determined that Claim 12 has not been infringed literally or under the doctrine of equivalents, dependent Claims 13 and 14 are likewise not infringed and will be included within the Court's grant of summary judgment in favor of Nintendo.

3. Claims 12-14 of the '899 Patent **Are Invalid**

Nintendo assets that Claims 12-14 of the '899 patent are invalid as anticipated by prior art not considered by the Patent Office. Specifically, Nintendo points to a Japanese patent application, Sharp II, which Nintendo asserts anticipated Claims 12-14. The invention disclosed in the Sharp II application was published on September 3, 1975, more than one year prior to the December 6, 1976 filing date of the '899 patent application. Sharp II was not disclosed to the Patent Office by the inventor in the prosecution of the '899 patent and not listed as a cited reference.

[19] To determine under s. 102(b) whether the RF switch disclosed in the '899 patent is anticipated by the automatic RF switch disclosed in the Sharp II application, the Court must undertake the three-step analysis

set out above in section I.E.

The first step is construction of the '899 patent claims to determine their meaning in light of the specification and prosecution history. Much has been discussed about claim construction in the infringement analysis of this Opinion. For purposes of the invalidity discussion, the Court will adopt an amendment to the '899 patent application filed by RCA Corporation with the Patent Office on October 4, 1977. In that amendment, the patentee described the '899 structure included in Claims 12-14 as a "potential responsive" RF switch, *i.e.*, the switching occurs in response to turning the power supply to the video record player "on" or "off." *See* Mascaro Cert. Ex. 9 at 76.

The second step of the inquiry requires the Court to compare Claims 12-14 with the subject matter described in Sharp II and identify the corresponding elements contained therein. But for the description of the invention disclosed in Sharp II, "Monitor Device for an Item Such as a Magnetic Recording Playback Device," every element of Claims 12-14, and every function used to accomplish the switching is taught in Sharp II. *See* Roberge Cert. para. 47 and Ex. F. Additionally, the means-plus-function elements of Claims 12-14 of the '899 patent are disclosed in Sharp II. Moreover, in Exhibit M to Roberge's Certification, he has prepared a claim chart which explains in detail the correspondence between the means-plus-function elements of each patent. FN16 In both patents the signal path between the antenna and television receiver reacts the same, subject to whether the power to the player is turned on or turned off. *See* Roberge Cert. para. 4. Similarly, the RF switches described and claimed in the '899 patent and Sharp II each perform the switching functions based on the presence or absence of power from the power supply. *See* id. para. 53.

FN16. Exhibit M to Roberge's Certification is attached hereto and designated as Appendix 3.

Because Sharp II discloses an automatic switch with corresponding elements to the '899 patent and the structure of Sharp II is equivalent to that of the '899 patent, the second step of the three-step analysis has been completed in favor of invalidity.

[20] The third and last step of the anticipation analysis requires the Court to determine whether the Sharp II reference is enabling, placing the allegedly disclosed matter in the possession of the public. In order for the RF switch disclosed in Sharp II to anticipate the RF switch in the '899 patent, one with ordinary skill in the art must be able to produce the invention described in the patent. *See* Akzo N.V. v. United States Int'l Trade Comm'n, 808 F.2d 1471, 1479 (Fed.Cir.1986), *cert. denied,* 482 U.S. 909, 107 S.Ct. 2490, 96 L.Ed.2d 382 (1987). Prior art references are presumed to be enabling. *See* In re Sasse, 629 F.2d 675, 681 (C.C.P.A.1980). Therefore, GE bears the burden of proving that the Sharp II reference was not enabling.

GE's expert, Wallace, attempts to differentiate between the power being given to Sharp II's magnetic recording/playback device and the power supply voltage in the '899 patent, and concludes that the Sharp II reference would describe an inoperable device having unnecessary components. *See* Wallace Cert. para. 80. Moreover, because of these differences, he determines that Sharp II does not disclose elements (5) and (6) of Claim 12 enumerated in the '899 patent. *See* id.

Based on this analysis, GE concludes that "when the Sharp II reference states that 'power is given to the magnetic recording/playback device,' " it really means that the "VCR is played in the play mode," and that there is no switching between RF signal paths until the VCR is placed in the play mode. GE's Br. in Opp. at 36; Wallace Decl. para. 76. GE's premise overlooks a later description of a specific embodiment found in Sharp II:

Furthermore, as is noted in the example reduced to practice, if it is provided with a relay coil that excites *simultaneously with the power being given to the magnetic recording/playback device* and is made so that

with this relay switch it performs *simultaneously the adding of bias to the signal switch to the television receiver* and the variable capacitance diodes, [and] general diodes, *this switching operation is performed completely automatically* and is extremely beneficial.

Roberge Cert. Ex. F at 3-4 (emphasis added).

It is plain from this reference that in this preferred embodiment of Sharp II, switching occurs when power is applied to the entire recording/playback device. No mention of any limitation related to a "play mode" is found anywhere in Sharp II. *See* id.; Nintendo's Reply Br. at 12.

In its invalidity argument, Nintendo has successfully countered all of GE's arguments that belie the invalidity of Claims 12-14 of the '899 patent. In accord with the requisite three-step analysis, the Court finds by clear and convincing evidence that Sharp II anticipates '899 patent Claims 12-14. No genuine issue of material fact exists and summary judgment on this ground is likewise appropriate.

III. UNITED STATES PATENT NO. 4,169,659

A. Background

United States Patent No. 4,169,659 (the " '659 patent"), entitled "Multiple Standard Television Sync Generator," was issued by the Patent Office on October 2, 1979. *See* Lechner Decl. Ex. B (copy of '659 patent).FN17

FN17. Nintendo includes a copy of the '659 as patent Exhibit A to the certification of its expert, Steven Mayer.

1. Sync Generators

The '659 patent relates to a television synchronization signal generator (a "sync generator") that provides a variety of signals needed to produce a picture on a television. A television signal is a combination signal that includes video information and encoded timing information necessary to produce a picture. Any device that is used to cause a picture to be displayed on a television set (*e.g.,* television cameras, video tape recorders, video game systems) requires a sync generator to produce signals that the television can understand and use.

A television signal transmitted to a television from a television camera is generated using an electron scanning beam inside the camera. The lens of the camera first focusses light from the captured image onto the camera's light sensitive faceplate. The electron beam inside the television camera then scans or "reads" the image off the faceplate. The camera's reading is done in a way that resembles the way one reads a page of text. The beam begins reading at the top left corner of the faceplate, reads a line from left to right, and then shuts off (or "blanks") and quickly returns to the left side to read the next line. This process continues until the beam reaches the bottom of the faceplate, at which time the beam shuts off (blanks) and quickly moves back to the top and repeats the process. The circuits that deflect the electron beam from left to right and down to up are known as "deflection circuits."

As the camera's scanning beam reads the image, the intensity of the beam is varied in accordance with the intensity of the light striking the faceplate. Picture signals representing the image being captured are then created in the camera on the basis of these variations. *See* Mayer Cert. para.para. 10-11; Lechner Decl. para. 7.

These picture signals are subsequently transmitted by the television camera to a television. *See* Mayer Cert.

para. 18. A separate electron scanning beam in the television reacts to the video and timing information in the composite television signal and electronicallyscans or "paints" an image on the television screen. The television's beam paints the picture in much the same way as the camera reads the picture-line-by-line, from left to right. The television beam paints thirty full frames each second, at which rate the human eye views the image on the television screen as uninterrupted. *See* Lechner Decl. para. 7.

Sync generators are used to control precisely the motion of the electron beam in a television camera and to coordinate that motion with the picture video information that is sent to the television. *See* Mayer Cert. para. 13. A television camera's sync generator generates three different types of signals: blanking, sync and drive signals. Blanking signals are used by both the camera and the television set and turn off or blank out the electron scanning beam when it is returning from right to left or from bottom to top of the camera's faceplate or television's screen. *See* Mayer Cert. para. 15. Sync signals are used by the television set to control the motion of the television's electron beam so that it moves synchronously with the camera's beam. *See* id. para. 17. Sync signals also provide other necessary information relating to the positioning of video information on the picture screen (such as "color burst" signals and "field identity" signals, among others). *See* GE's Br. in Opp. at 1. Blanking and sync signals indisputably are part of the composite television signal sent from a camera to the television. Drive signals, at the very least, are applied to the deflection circuits inside the camera, thereby controlling the horizontal and vertical motion of the electron scanning beam inside the camera.FN18

FN18. Whether "drive signals," as defined in the '659 patent, include signals that are sent from the camera to the television is a central issue here and will be discussed below.

Because the above signals have to synchronized, digital systems such as that claimed in the '659 patent contain an electronic circuit called a "clock." The clock generates a uniform series of electrical pulses that synchronizes the operations and data transfers that take place among the components in the system. *See* Mayer Cert. para.para. 22-23.

As discussed below, Claim 1 of the '659 patent is limited to a sync generator that includes a "vertical counter" that is "clocked by a signal which is advanced in phase." A "counter" is an electronic circuit that counts the number of clock pulses it receives. A counter is built with several individual memory elements, called "flip-flops," which collectively keep track of the number of pulses the counter has received and counted. Each time the counter receives a pulse, the binary states (*i.e.*, either a zero or a one) of some or all of its flip-flops change and collectively represent the next highest value of the counter. The states of the flip-flops can be examined by other electronic circuits in the system to determine the number of pulses that the counter has counted. *See* id. para.para. 22-26; Blank Cert. Ex. 3 at 56, lines 9-23; 57, line 9 to 58, line 9.

Each of the individual flip-flops in a counter has a "clock" input which receives the clock signal that puts each flip-flop into its next state. A flip-flop can only be put into its next state when a signal at its clock input is received, and it is therefore said to be "clocked by" that signal. *See* Mayer Cert. para. 27; Blank Cert. Ex. 3 at 57, line 23 to 58, line 9; 59, lines 15-20; 71, line 4 to 72, line 2.

Counters are generally one of two types-synchronous or non-synchronous (also called "asynchronous"). In a synchronous counter, an input pulse to be counted is applied to the clock inputs of each of the individual flip-flop elements simultaneously. Thus, all of the flip-flops receive the input pulse and are put into their next state simultaneously. Accordingly, there is very little delay between application of an input pulse to the counter and the counter's transition to its next highest value. *See* Mayer Cert. para. 29 and Ex. D at 1; Blank Cert. Ex. 3 at 56, line 24 to 57, line 8; 58, line 20 to 59, line 14; 73, lines 3-16; 77, line 23 to 78, line 9; 80, lines 5-20; 97, line 20 to 98, line 18.

In a non-synchronous counter, a pulse to be counted is connected only to the clock input of the first flip-flop. An output of that flip-flop is in turn connected in series to the clock input of the second flip-flop, and so on, so that each flip-flop is clocked by an output of the flip-flop immediately before it. Thus, in a non-synchronous counter, no flip-flop can go into its next state until the flip-flop immediately before it has done so. Thus, the flip-flop transitions occur sequentially, one at a time. With this construction, the delay between the application of an input pulse to the counter and the counter's transition to its next highest value is relatively long, since it takes time for that input pulse to "ripple through" all of the counter's flip-flops. This delay, which is called "propagation delay," is inherent in non-synchronous counters. *See* Mayer Cert. para. 30 and Ex. D at 2; Blank Cert. Ex. 3 at 63, line 3 to 64, line 3; 65, lines 8-23; 79, line 19 to 80, line 4; 95, line 23 to 97, line 19.

A synchronous counter is said to be "clocked by" the signal supplied to the clock input of all its individual flip-flops. A non-synchronous counter is said to be "clocked by" the signal supplied to the clock input of its first flip-flop. *See* Mayer Cert. para.para. 29-30; Blank Cert. Ex. 3 at 62, lines 8-24; 65, line 8 to 66, line 8; 72, lines 3-25.

2. The '659 Patent

Turning to the specific nature of the parties' dispute, GE has asserted Claims 1, 3, 4, 5 and 13 of the '659 patent against Nintendo's SNES video game system. Claim 1 is an independent claim that provides as follows, with the claim language at issue underlined:

1. A television synchronizing signal generator, comprising:

a source of clock pulses;

a synchronous horizontal counter responsive to said clock pulses from said source for producing signals having integral multiples of the horizontal line frequency of the television signal;

a vertical counter coupled to an output of said synchronous horizontal counter for producing signals having frequencies which are integral divisions of twice the line frequency of the television signal, *said vertical counter being clocked by a signal which is advanced in phase relative to the lowest frequency signal produced by said synchronous horizontal counter;*

output means for generating blanking, sync and *drive signals;*

gating means coupled to said synchronous horizontal counter and said vertical counter for conditioning said output means for the generation of said blanking, sync and *drive signals;* and

means for rendering said output means responsive to said clock pulses so that said blanking, sync and *drive signals* are phase-related to said clock pulses.

Lechner Decl. Ex. B. at col. 18, lines 40-64 (emphasis added).

Claim 3 is dependent on Claim 1; thus, Claim 3 incorporates all of the limitations of Claim 1. Claim 4 is another independent claim, on which Claims 5 and 13 are dependent; thus, Claims 5 and 13 incorporate all of the limitations of Claim 4. The claim limitations at issue here, "drive signals" and "said vertical counter being clocked by a signal which is advanced in phase relative to the lowest frequency signal produced by said synchronous horizontal counter," are found both in Claim 1 and Claim 4 and are the same in each claim. FN19 As such, the Court will focus its discussion on the limitations highlighted above in Claim 1, with the understanding that those limitations are at the heart of GE's allegations of infringement under each

of Claims 1, 3, 4, 5 and 13.

FN19. Independent Claim 4 provides:

4. A multiple standard television synchronizing signal generator comprising:

a source of clock pulses which provides pulses at a first rate for a 525-line sync standard and at a second rate or a 625-line sync standard;

means for programming the synchronizing signal generator for operation according to a selected sync signal standard and having a first input terminal for selecting a particular horizontal line frequency and a second input terminal for selecting a particular sync signal standard;

a synchronous horizontal counter responsive to said clock pulses from said source for producing signals having frequencies which are integral multiples of the selected horizontal line frequency;

a vertical counter coupled to an output of said synchronous horizontal counter and programmed by said programming mean for operation at a selected horizontal line frequency for producing signals having frequencies which are integral divisions of twice the horizontal line frequency, *said vertical counter being clocked by a signal which is advanced in phase relative to the lowest frequency signal produced by said synchronous horizontal counter;*

output means for generating blanking, sync and *drive signals* of the selected sync signal standard;

gating means coupled to said programming means, said synchronous horizontal counter and said vertical counter for conditioning said output means for the generation of blanking, sync and *drive signals;* and

means for rendering said output means responsive to said clock pulses so that said blanking, sync and *drive signals* are phase-related to said clock pulses.

Lechner Decl. Ex. B. at col. 19, lines 10-44.
As indicated by the underlined portions of Claim 1 above, the '659 patent speaks of a sync generator that (1) generates "drive signals" and (2) contains a vertical counter that is "clocked" by a signal which is "advanced in phase." The parties dispute the precise meaning and scope of these claim limitations and, consequently, are before the Court today.

To ascertain the meaning of these limitations, the Court will necessarily have to look at, *inter alia,* the '659 specification. While Claim 1 does not explicitly limit use of the '659 patent to any one component of television equipment, the specification focusses on using the '659 patent within a television camera and uses a television camera as the preferred embodiment of the patent. *See, e.g.,* Lechner Decl. Ex. B at col. 1, lines 38-46. The specification also references signals produced by a sync generator when used in a video tape recorder. *See* id. at col. 7, lines 50-61. The uses of a sync generator are highlighted at the outset of the specification:

The present invention relates generally to television sync generators, and particularly to a novel television sync generator which is programmed to provide one of a plurality of standard synchronization signals.

A synchronizing signal generator is used in a television camera to control the horizontal and vertical drive and the horizontal and vertical blanking of the electron beam so that a composite TV picture is produced by the camera. Sync generators are also used in video tape recorder systems for producing a recorded composite video signal from a source of color signals, and to produce a duplicate video tape from an existing video tape.

Id. at col. 1, lines 5-16.FN20

FN20. The true novelty of the '659 patent was its ability to generate a television signal that was compatible with any of the four main television standards throughout the world. Prior to the '659 patent, when broadcast equipment was to be constructed for operation in a country employing a different television standard, the sync generator had to be redesigned and reconstructed to be compatible with the different standard. *See* Lechner Decl. Ex. B at col. 1, lines 17-37.

a. Drive Signals

With respect to drive signals, the specification establishes the following: "The HORIZONTAL DRIVE/CHROMA signal is produced during each horizontal synchronizing interval and is used to trigger the horizontal deflection system *in the television camera*. The HORIZONTAL/CHROMA signal is also used in the SECAM system to blank the chroma signal *in the camera* at the beginning of each horizontal line." Id. at col. 6, lines 56-63.FN21 The specification also states: "The VERTICAL DRIVE signal is used to trigger the vertical deflection circuitry *in a television camera*." Id. at col. 7, lines 44-46. The specification includes no other definition of drive signals.

FN21. Whether moving from left to right or from top to bottom, the electron scanning beam inside the television camera is controlled by magnetic forces created by magnets located inside the television camera. A camera has both a horizontal magnet and a vertical magnet. When the beam reaches the right or bottom of the faceplate, a drive signal created by the sync generator neutralizes the respective magnetic force, such that the beam returns (or is deflected) to the left or top of the faceplate. The horizontal deflection system is the system inside a television camera that causes the electron scanning beam to return from the right end of a horizontal line to the left end of the next horizontal line. The vertical deflection system causes the same result with respect to the electron scanning beam returning from the bottom of the faceplate to the top.

b. Vertical Counter Clocked by Signal Advanced in Phase

The sync generator described and claimed in the '659 patent includes a "horizontal" counter and a "vertical" counter. The horizontal counter monitors the horizontal motion of the electron beam, with the counter's value representing where on a horizontal line the beam is located at a given time. The vertical counter monitors the beam's vertical motion, with its value representing the line on which the beam is operating. The output signals from the individual flip-flops of both of these counters are coupled to "decoder circuitry" which, on the basis of the values of the counters, generate blanking, sync and drive signals at the appropriate times. *See* Lechner Decl. Ex. B at col. 7, line 62 to col. 8, line 24; *see also* Mayer Cert. para. 51; Blank Cert. Ex. 3 at 121, line 24 to 122, line 11.

To reduce the complexity and number of components, while still permitting its sync generator to operate

with the various worldwide television standards, the '659 patent contemplates a non-synchronous vertical counter, despite the timing problems such counters can cause because of their propagation delay. *See* Lechner Decl. Ex. B at col. 2, lines 31-34; col. 11, lines 3-22; *see also* Mayer Cert. para.para. 52-54; Blank Cert. Ex. 3 at 65, line 24 to 67, line 3; 68, line 16 to 69, line 2; 89, lines 3-20; 103, lines 11-21. To overcome these timing problems, the circuitry described in the '659 patent sends a "phase advanced signal" to the clock input of the non-synchronous vertical counter well before its output signals are needed to determine the vertical position of the electron beam.

This phase advanced clocking gives the non-synchronous vertical counter a "head start," which allows sufficient time for the clock pulse to "ripple through" each stage of the counter. This head start ensures that the vertical counter will have been fully incremented by the time the decoder circuitry examines the vertical counter's outputs after each horizontal line. *See* Lechner Decl. Ex. B at col. 3, lines 47-55; col. 11, lines 40-55; *see also* Mayer Cert. para.para. 54-58; Blank Cert. Ex. 3 at 89, line 21 to 91, line 9; 103, lines 11-21.

In the '659 patent specification, the horizontal counter is a synchronous counter. *See* Lechner Decl. Ex. B at col. 2, lines 15-20. The horizontal counter counts the clock pulses and outputs a signal called "2H" each time the horizontal counter reaches its maximum count of 63. *See* id. at col. 10, lines 5-44; Fig. 3. On the next pulse, the horizontal counter returns to zero, so that it can count the next sequence of pulses it receives. *See* id. at col. 9, lines 48-51.

In terms of the claim language of the '659 patent, the vertical counter is "clocked by a signal which is *advanced in phase* relative to the lowest frequency signal produced by said synchronous horizontal counter." *See* id. at col. 18, lines 52-55 (emphasis added). The "lowest frequency signal" to which the claim refers is the 2H signal from the horizontal counter, which occurs at count 63 before the counter is reset to zero. The signal that is used to clock the non-synchronous vertical counter is called "ADVANCE." The ADVANCE signal recurs at the same frequency as 2H, but is "advanced in phase" relative to the 2H signal because it begins on pulse 56, seven clock pulses before the 2H signal. *See* id. at col. 11, lines 12-14 and 32-35.

In terms of the timing signals produced by the '659 sync generator, the ADVANCE signal is supplied to the vertical counter before any of the horizontal timing signals (which turn the electron beam off and reposition it) are produced at the end of a horizontal line. Accordingly, the vertical counter has settled out and incremented its count while the electron beam is still moving across a horizontal line and is ready to be "read" by the decoder circuitry at the end of each horizontal line. *See* Mayer Cert. para.para. 60-61; Blank Cert. Ex. 3 at 89, line 21 to 91, line 9; 137, lines 10-16.

3. Nintendo's Denial of Infringement

Nintendo denies that the sync generator in its SNES system infringes the '659 patent. Nintendo advances two arguments in support of its claim of non-infringement: (1) the SNES does not generate drive signals, as claimed by the '659 patent; and (2) the SNES does not use an advanced in phase signal to clock its vertical counter, as claimed by the '659 patent.

a. Nintendo's SNES Sync Generator

As set forth in Nintendo's brief in support of its motion for summary judgment, the SNES is a video game system that, like a television camera, outputs a composite television signal, which includes both video and timing information. In particular, the timing information comprises sync and blanking signals that are used by the television to control the television's electron beam motion. *See* Nintendo's Br. at 19; Mayer Cert. para.para. 62-63. Unlike a television camera, however, the SNES does not include a camera tube, a gun for generating an electron beam inside the camera or any other type of scanning device. *See* Nintendo's Br. at 19; Mayer Cert. para.para. 62 and 74. The SNES therefore has no need to generate drive signals to control

an electron scanning beam that "reads" images.

The SNES picture processing circuitry is contained on two custom chips called Picture Processing Units ("PPUs"). The two PPUs together generate the synchronizing and blanking signals output by the unit, and each PPU has a horizontal counter and a vertical counter. *See* Nintendo's Br. at 19. Each counter is synchronous. As a result, the same clock signal is fed to the clock inputs of all the flip-flops in both the horizontal and vertical counters in each PPU. Thus, Nintendo asserts, each counter is clocked by the same signal. *See* id. at 19-20.

The horizontal and vertical counters in the SNES are designed so that the horizontal counters are incremented by every clock pulse, while the vertical counters (although they receive every pulse) are incremented by a pulse only once per horizontal line. This is done by "enabling" the vertical counters to count (*i.e.,* turning the counters on) only when the horizontal counters have reached their maximum value. The vertical counters are then incremented by the next clock pulse at the same time the horizontal counters are reset to zero. *See* id. at 20.

Specifically, the horizontal counters are designed to count from 0-339 as the television's electron beam moves from the far left to the far right of the television screen. When the horizontal counter in the first PPU reaches a value of 338, a signal called "HCLD" is generated. This signal is stored in a special flip-flop in each PPU. On the next system clock pulse (the 339th), each of these special flip-flops sends a signal to the enable inputs of the vertical counters and to inputs of the horizontal counters which enable them to be reset to zero.FN22 *See* id.

FN22. The "enable" input of a counter is an input to which a signal is provided to "turn on" the counters to allow it to be incremented. *See* Mayer Cert. para. 32.

On the next clock pulse (the 340th), the vertical counters are incremented and the horizontal counters are reset to zero. The vertical counters are therefore incremented by the same system clock pulse which increments the horizontal counters from 339 (their maximum value) to zero.FN23 *See* id. at 20-21.

FN23. The special flip-flops that hold the HCLD signal for the vertical counters from count 338 to 339 are used to ensure that the vertical counters contained in the two PPU chips simultaneously receive an enable signal on clock pulse 339 so that they continue to operate in lock-step. Those flip-flops do not provide a signal to the clock inputs of the vertical counters, which continue simultaneously to receive clock pulses directly from the clock. *See* Mayer Cert. para. 71.

b. Nintendo's Arguments in Support of Non-Infringement Claim

Nintendo correctly avers that Claim 1 of the '659 patent requires a sync generator that includes "means" for generating, *inter alia,* "drive signals." Nintendo posits that, as explicitly defined in the '659 specification, drive signals trigger the horizontal and vertical deflection circuitry in a *television camera*. *See* Nintendo's Br. at 25. Nintendo asserts that this definition of drive signals is consistent with the term's ordinary meaning as understood by the relevant industry. *See* id. In essence, Nintendo argues that the '659 patent puts persons of ordinary skill on notice that the "drive signal" limitation is limited to a sync generator for use in a television camera and cannot be asserted against a video game system. *See* id. at 26.

Nintendo opines that "[b]ecause the SNES, unlike a television camera, does not contain an electron scanning beam, no ... 'drive signals' are ever needed, and, in fact, the SNES does not generate any drive signals." Id. at 25. Based on the above assertions, Nintendo concludes that "there is no Infringement as a matter of law

because the SNES does not generate drive signals as required by the asserted claims." Id. at 25-26 (citing Carroll Touch, Inc. v. Electro Mechanical Sys., Inc., 15 F.3d 1573, 1578 (Fed.Cir.1993); Intellicall, Inc. v. Phonometrics, Inc., 952 F.2d 1384, 1388-89 (Fed.Cir.1992); Johnston v. IVAC Corp., 885 F.2d 1574, 1579 (Fed.Cir.1989); Pennwalt Corp. v. Durand-Wayland, Inc., 833 F.2d 931, 934 (Fed.Cir.1987) (*en banc*), *cert. denied,* 485 U.S. 961, 1009, 108 S.Ct. 1226, 1474, 99 L.Ed.2d 426, 703 (1988)).

With respect to the signal supplied to the vertical counter of the SNES, Nintendo contends that it is not "advanced in phase." *See id.* at 27-31. Nintendo argues that because all of the counters in the SNES are synchronous and therefore receive the same clock pulses at their clock inputs at the same time, the signal supplied to the clock input of the vertical counters is "in phase" with the lowest frequency signal produced by the horizontal counters (the HCLD signal). *See id.* at 27. Because of this fact, Nintendo states, the vertical counters are incremented to their next value by the same clock pulse that increments the horizontal counters from 339 (their maximum value) to zero. *See id.* at 28. Thus, Nintendo concludes, the vertical counters are not clocked by an advanced in phase signal, and the SNES does not infringe the '659 patent.

As a final point, Nintendo addresses an anticipated argument from GE-that the SNES's HCLD signal, produced by the horizontal counter at pulse 338 and sent to the enable input of the vertical counter on pulse 339, is the relevant advanced in phase signal. Nintendo first exclaims that the use of enabling signals to allow a counter to count clock pulses is common and pre-dates both the '659 patent and the SNES. *See* id. at 28 (citing to Mayer Cert. Ex. K (1976 copy of Texas Instruments Data Book for Design Engineers which displays use of enabling circuitry in synchronous counters)). Next, Nintendo argues that the SNES enable signal is not a signal which "clocks" the vertical counter; rather, the SNES enable signal merely "turns on" the vertical counter to enable it to be incremented when it receives the next clock pulse supplied to its clock input.FN24 *See* id. at 30. Nintendo insists that the SNES vertical counter is only "clocked" when it receives a pulse at its clock input. *See* id.

FN24. Nintendo also explains that the HCLD signal in the SNES serves an entirely different purpose than the ADVANCE signal in the '659 patent: "In contrast to the SNES's HCLD signal, which is designed to ensure lock-step operation of the synchronous counters in each of the two PPU chips, the phase advanced signal in the '659 patent ... is used to compensate for the delay problems which arise from using a non-synchronous vertical counter." *See* id. at 30 n. 14.

In support of this position, Nintendo highlights testimony from Dr. Frank Marlowe, the inventor of the '659 patent, who stated that supplying a signal to the enable input of a counter does not "clock" the counter. *See* id. (citing Blank Cert. Ex. 3 at 73, lines 2-13). Dr. Marlowe also indicated that the only way of which he was aware to "clock" a synchronous counter was to supply the clock signal simultaneously to the clock inputs of each of the flip-flops inside the counter. *See* Blank Cert. Ex. 3 at 72, lines 3-25.FN25

FN25. Nintendo also briefly argues that, even if the HCLD signal was the relevant signal, it is not advanced in phase. *See* Nintendo Br. at 31.

As summarized by Nintendo: "Because the vertical counters in the SNES are clocked by the same signal that clocks the horizontal counter, and not by a signal that is 'advanced in phase,' the SNES does not literally infringe the asserted claims of the '659 patent." Nintendo's Br. at 31.

With respect to the doctrine of equivalents, Nintendo asserts the above arguments as evidence that the SNES and '659 patents are substantially different. Nintendo also voices two additional thoughts of non-equivalence. First, Nintendo states that the '659 patent is different because the '659 vertical counter receives the phase advanced signal and begins to change state while the electron beam is still scanning a horizontal

line. In the SNES, the vertical counter changes state after the beam is done scanning a horizontal line, at the exact moment the beam is repositioning to start another line. Second, Nintendo asserts that GE cannot invoke the doctrine of equivalents because to do so would run afoul of the rule that the doctrine cannot be used to claim subject matter in, or obvious in light of, prior art. *See* id. at 33. Nintendo contends that the SNES is akin, in relevant respects, to a prior art sync generator disclosed in Dr. Marlowe's Ph.D. thesis in which the advanced in phase signal was sent to the vertical counter *after* horizontal timing signals had begun, *i.e.,* after the beam had finished scanning a horizontal line. *See* id. (citing Blank Cert. Ex. 3 at 417, line 12 to 419, line 3).

4. GE's Reply to Nintendo's Non-Infringement Analysis

GE argues that the each of the elements of Claim 1 of the '659 patent are found in the SNES. GE's opposition to Nintendo's motion for summary judgment is rooted in conceptual differences as to the meaning of "drive signals," as used in the '659 patent, and as to whether the SNES utilizes an "advanced in phase" signal to clock its vertical counter.

a. Drive Signals

At the outset of its argument against granting summary judgment, GE asserts that the plain language of the patent claims require only "drive signals," not "drive signals that are used to control the electron beam in a television camera." *See* GE's Br. in Opp. at 16. GE contends that Nintendo wrongly tries to import the additional "television camera" limitation into the claims from the preferred embodiment disclosed in the '659 patent specification. *See* id. GE avers that the Federal Circuit has condemned incorporating a limitation from the specification into the claims. *See* id. at 16 and 19 (quoting SRI Int'l v. Matsushita Elec. Corp. of Am., 775 F.2d 1107, 1121 and n. 14 (Fed.Cir.1985) (*en banc*)). GE also insists that the specification does not discuss only television cameras, but video tape recorders as well. *See id*. at 17. As noted by Nintendo and highlighted by GE, video tape recorders have no electron scanning beam and, thus, do not require drive signals. *See id.;* Mayer Cert. para. 42 n. 5. GE concludes that because "the claims of the '659 patent nowhere mention a television camera, the only reasonable conclusion is that the term 'drive signal' as used in the claims was intended to have its common, broad meaning so that the claims would cover television cameras, video tape recorders and other sources of television signals that have need of a sync generator." Id. at 17-18.

GE also states that "[a]lthough certain of the specific drive signals described in the preferred embodiment are used inside a television camera, they are not the only drive signals described in the patent." Id. For example, GE contends that a separate signal disclosed in the '659 patent, the "Vertical Drive Interval," FN26 is a drive signal, is not used inside the television camera and is sent to the television as part of the composite television signal. *See* id. The Vertical Drive Interval signal is part of the composite sync signal. *See* Lechner Decl. para. 49.

FN26. The Vertical Drive Interval signal occurs inside the television during the vertical blanking interval, during which time the television's electron beam shuts off and repositions to the top of the screen. *See* Lechner Decl. para. 49.

As a second attack on Nintendo's argument with respect to "drive signals," GE asserts that persons of ordinary skill would not necessarily understand that term to be limited to television cameras. In support of this argument, GE highlights excerpts from two other patents, which appear to reference drive signals as being used to control the electron beam inside the television. *See* GE's Br. in Opp. at 19-21. In particular, GE discusses United States Patent No. 4,739,390 (the " '390 patent") (describing a "deflection drive signal" that controls the electron beam in a television) and United States Patent No. 4,282,549 (the " '549 patent") (same), which was issued the same year that the '659 patent was issued. *See* id.; Pollack Decl. Ex. F (the '390

patent) at col. 2, lines 14-15; Ex. H (the '549 patent) at col. 1, lines 5-8. On the basis of this asserted broader meaning of "drive signals," GE argues that the term encompasses signals other than those generated inside a television camera to control the camera's electron beam.

GE next asserts that the SNES produces drive signals-that is, signals that control the operation of the electron scanning beam in the *television* by triggering the horizontal and vertical deflection circuitry. *See* GE's Br. in Opp. at 21. GE contends that the composite sync signal produced by the SNES sync generator includes drive signal information used to control the television's electron scanning beam. *See* id. Thus, GE posits, the SNES produces drive signals as that term is used in the asserted claims of the '659 patent.FN27

FN27. GE also argues that the SNES produces other drive signals as claimed in the '659 patent. In particular, GE maintains that the SNES creates a signal, labeled CSSEA 1, that is analogous to the VERTICAL DRIVE INTERVAL signal produced by the '659 patent. Moreover, GE contends that the SNES signal called WINCLB is a drive signal because, like the Hdrive signal in the '659 patent, it indicates to the SNES picture generation circuitry that the next line of information is to be assembled. *See* GE's Br. in Opp. at 22-23.

b. Vertical Counter Clocked by Signal Advanced in Phase

With respect to the vertical counter and whether it is "clocked" by a signal that is "advanced in phase," GE's central argument in opposition to Nintendo's claim of non-infringement is that the SNES' HCLD signal is the signal that "clocks" the vertical counter. *See* id. at 26-27. This proposition is contrary to Nintendo's assertion that the SNES' vertical counter is clocked by the system clock signal-the same signal that clocks the horizontal counter. GE contends that because the HCLD signal, which is undisputedly advanced in phase, clocks the SNES vertical counter, the SNES infringes the '659 patent.

GE also takes issue with several subsidiary arguments put forth by Nintendo. First, GE disregards as irrelevant Nintendo's observation that the '659 vertical counter "begins to change state while the beam is still scanning a horizontal line." *See* id. at 25 n. 9 (quoting Nintendo's Br. at 33). GE contends that the asserted claims require only that the "advanced in phase" signal be sent prior to "the lowest frequency signal" produced by the horizontal counter. Whether the beam is still scanning, GE opines, is meaningless. Second, GE rejects, again as irrelevant, Nintendo's discussion concerning alleged differences between synchronous and non-synchronous counters. GE argues that Claim 1 does not require a non-synchronous counter, both synchronous and non-synchronous counters exhibit some propagation delay, and the '659 patent could have used either type of counter. *See* id. at 25.

c. Doctrine of Equivalents

GE argues that if the Court were to determine that the SNES does not literally satisfy the "drive signals" or "advanced in phase" elements of the '659 patent claims, genuine issues of material fact exist under the doctrine of equivalents. First, GE states that, even if "drive signals" was limited to television cameras, the SNES produces signals that operate in the same manner as drive signals inside a television camera, *i.e.*, to notify the picture gathering circuitry when the next line of horizontal picture information is to be collected. *See* id. at 30-31. Second, GE repeats that whether a synchronous or non-synchronous vertical counter is utilized is irrelevant; under the '659 patent, the two are interchangeable. *See* id. at 31. Finally, GE argues that Nintendo's prior art argument is unfounded both legally and factually. *See* id. at 31-33.

5. Expert Testimony

a. Steven Mayer for Nintendo

Steven Mayer ("Mayer") has over 35 years experience as an electrical and design engineer in the television and video game industries. He was one of the founders of Atari, which became the largest manufacturer of video games in the late 1970's and early 1980's, and later worked as president of Warner Communications Laboratories and founded Digital F/X, a designer and manufacturer of video work stations for the television and film industry. Mayer has been retained by Nintendo. *See* Mayer Cert. para.para. 1-4.

Mayer has studied (1) the '659 patent, (2) its prosecution history, (3) the prior art reference cited during the prosecution of the '659 patent, (4) the relevant sections of the SNES Development Manual and logic level schematics of the synchronizing circuitry in the SNES, (5) a number of prior art references that were not before the Patent Office when it examined the '659 patent, (6) the deposition transcript and exhibits of Dr. Marlowe, the inventor of the '659 patent, and (7) various documents produced by GE and third parties to Nintendo. See id. para. 5.

Mayer concludes that the SNES does not infringe any of the asserted claims of the '659 patent for two reasons: (1) the '659 patent defines "drive signals" as signals which control the scanning beam in a television camera and the SNES has no means for producing such drive signals; and (2) the vertical counter used in the SNES synchronizing circuitry is not clocked by a phase advanced signal. *See* id. para. 6.

In paragraphs 8-32 of his certification, Mayer discusses certain background information on the use of sync generators in traditional television cameras and the design and operation of sync generators. Much of that information is set forth above. With respect to sync generators used in television cameras and the signals produced thereby, Mayer summarizes his testimony as follows:

[T]elevision cameras use sync generators, which create drive signals at the end of each sweep of the camera's electron beam to trigger the horizontal and vertical deflection circuits in the camera and control the movement of the scanning beam of the camera. Television camera sync generators also create blanking and sync signals for use by the television set in projecting an image onto a television screen.

Id. para. 21.

With respect to vertical counters, Mayer provides general information and notably avers that a counter's "flip-flop is said to be 'clocked by' the signal supplied to its clock input." Id. para. 27. "The mere presence of an enable signal cannot increment a counter. [A counter] can only be incremented by a pulse received at its clock input." Id. para. 32.

In paragraphs 33-44 of his certification, Mayer discusses some of the prior art and the use of sync generators in video games. Mayer first establishes that a person of ordinary skill in the art at the time the '659 patent was filed in May 1977 would have understood "drive signals" to refer to those signals that trigger the deflection circuits inside a television camera. *See* id. para. 48. In support, Mayer refers to a 1949 text entitled *Basic Television-Principles and Servicing,* written by Bernard Grob. In that text, Grob described a sync generator that produced drive signals to synchronize the deflection circuitry in a television studio camera. *See* Mayer Cert. para. 36 and Ex. E at 523-31. Mayer also refers to a sync generator chip manufactured by Fairchild Semiconductor in 1972 which generated blanking, sync and drive signals using synchronous digital counters. Documents relating to that chip show that drive signals are sent only to the deflection circuits in the camera to control the camera's scanning beam, while a composite television signal, including a "composite sync" signal, is sent from the camera to the television. *See* id. para. 37 and Ex. F. Finally, Mayer references another sync generator integrated circuit chip, which operated similarly to the Fairchild chip. *See* id. para. 38 and Ex. G.

As to the use of sync generators inside a video game, Mayer testifies that video games require sync generators to produce blanking and sync signals. Video games, however, are not television cameras; they

generate synthetic video images and do not capture live images. Thus, Mayer declares, video games have no electron beam, no deflection circuits and no need for drive signals. *See* id. para.para. 2 41-43.FN28

FN28. Mayer acknowledges that video tape recorders became popular in the 1970's and usually had sync generators to produce the blanking and sync signals needed for the television. Mayer also states, however, that, like video games, video tape recorders have no scanning beam and no need for drive signals. *See* Mayer Cert. para. 42 n. 5.

In paragraphs 45-61 of his certification, Mayer discusses the "drive signal" and "vertical counter being clocked by a signal which is advanced in phase" elements of Claim 1 of the '659 patent. As to "drive signals," Mayer labels the '659 patent a "television camera sync generator," and highlights the definitions of drive signals from the '659 specification, which expressly state that the drive signals are used to trigger the deflection circuitry *in the television camera*. *See* id. para.para. 45-47. Mayer asserts that this use of drive signals is consistent with the manner that one of ordinary skill in the art would have used it. *See* id. para. 48 (quoting three texts dated 1971 or earlier). Mayer also cites to certain diagrams drawn by Dr. Marlowe, which Mayer asserts show that Dr. Marlowe understood the ordinary use of drive signals as limited to television cameras. *See* id. para.para. 49-50.

As to the vertical counter, Mayer quotes the '659 specification which acknowledges the inherent propagation delay problems with non-synchronous counters and explains that the '659 patent nonetheless uses a non-synchronous counter because it is less complex and has fewer components than a synchronous counter. *See* id. para.para. 51-54. To compensate for the delay problems, Mayer observes, the '659 patent uses an advanced in phase signal that begins to ripple through the non-synchronous vertical counter before the horizontal counter reaches its maximum count. *See* id. para. 54 (quoting Lechner Ex. B at col. 2, lines 26-34). The vertical counter receives the advanced in phase signal at its clock inputs. *See* id. para. 57. Mayer explains that this advanced signal technique ensures that, by the time the outputs of the vertical counter are examined-at or shortly after the horizontal counter is reset to zero-the vertical counter will have made the full transition to its next state. *See* id. para. 60. To ensure this, the vertical counter is clocked on count 56 of the preceding cycle, eight clock pulses before the beginning of the next horizontal cycle. *See* id. Thus, the vertical counter is clocked while the beam is still scanning the horizontal line. *See* id. para. 61.

In paragraphs 62-83 of his certification, Mayer discusses the SNES and explains why it does not infringe the relevant elements of the '659 patent claims. In describing the structure of the SNES sync generator, Mayer emphasizes that the SNES has no electron scanning beam and no need for drive signals. *See* id. para.para. 62, 73-75. Mayer also testifies that the SNES does not perform any function nor accomplish any result equivalent to the drive signals of the '659 patent. *See* id. para. 75.

As to the structure of the counters in the SNES, Mayer emphasizes that all the counters are synchronous and are clocked by the same signal. *See* id. para. 64. Mayer insists:

The SNES vertical counters are not clocked by their enable signal, because applying a signal to the enable inputs of the counters will neither increment the counters, nor put the flip-flops of the counters into their next states. The SNES vertical counters can only be incremented by signals applied to their clock input terminals. For this reason, a counter's "clock" input is fundamentally different from its "enable" input.

Id. para.para. 66-67.

Mayer also points out that "[i]n contrast to the vertical counter of the '659 patent, which is clocked by the phase-advanced signal *before* any of the horizontal timing signals are generated [*i.e.,* during a horizontal line scan], the vertical counters in the SNES are incremented well *after* any of the horizontal timing signals

begin [*i.e.,* after a horizontal line scan]." Id. para. 69. Mayer asserts that, unlike the '659 patent which examines the state of its vertical counter only at the beginning of each horizontal cycle, the SNES synchronizing circuitry examines the state of its vertical counter at many points, while the television beam is still scanning a horizontal line. Indeed, Mayer maintains, Dr. Marlowe testified that the distinction between incrementing the vertical counter before and after the horizontal timing signals was the main difference between the '659 patent and the prior art. *See* id. para. 81 (citing Blank Cert. Ex. 3 at 417, line 14 to 418, line 24).

Mayer testifies that if the SNES vertical counter was clocked during a horizontal line scan, problems would occur. *See* id. para. 70. Mayer states that the vertical counter is clocked by the same clock pulse that resets the horizontal counter to zero. *See* id. para. 77. Thus, Mayer explains, the SNES vertical counter is clocked by a signal that is "in phase" with the lowest frequency signal produced by the horizontal counter. *See* id. As such, Mayer concludes that the "vertical counters in the SNES are not clocked by a phase advanced signal or anything equivalent thereto ... [T]he SNES does not infringe the asserted claims of the '659 patent." Id. para. 83.

b. Bernard Lechner for GE

Bernard Lechner ("Lechner") has been an engineer in the field of television related electronics for more than 30 years. During the years 1957 through 1987, he held a variety of research and management positions at RCA's David Sarnoff Research Center, where he was responsible for the research and development of equipment for displaying and processing television signals. Lechner has been retained by GE. *See* Lechner Decl. para.para. 1-3.

Lechner has examined (1) the '659 patent, (2) its file history, (3) the SNES, and (4) various documents produced by Nintendo that describe the SNES. Based on his examination, Lechner concludes that the SNES incorporates each element of Claims 1, 3, 4, 5 and 13 of the '659 patent. Lechner asserts that the SNES infringes the '659 patent because, like the '659 patent, the SNES (1) produces blanking, sync and drive timing signals that are used in creating the composite television signal to control the scanning system of the television, and (2) generates its timing signals by using vertical counter circuitry that is clocked by a signal which is advanced in phase with respect to the lowest frequency signal produced by the horizontal counter circuitry. *See* id. para. 4.

In paragraphs 5-25 of his declaration, Lechner discusses background information relating to timing signals produced by sync generators; his conclusion is that the term drive signals means more than simply the signals that control a television camera's scanning beam. Lechner's background discussion is broader than Mayer's because it goes beyond just television cameras and discusses more thoroughly the timing signals in the composite television signal that the television uses to accurately reproduce the picture it receives.

Lechner describes a television signal as comprising, in part, (1) horizontal synchronization ("Hsync") pulses, which cause the television scanning beam to return to the left side of the screen, (2) color burst signals, which enable the television to add color to the television display, and (3) picture information. *See* id. para. 13. The Hsync and color burst signals occur during the horizontal blanking interval, during which time the scanning beam is turned off and returns to the left side of the screen. *See* id.

Other signals control the television's beam during the time period during which the beam is turned off and returns to the top of the screen. This time period is known as the Vblank interval. *See* id. para. 15. During the Vblank interval, vertical synchronization ("Vsync") pulses appear, which cause the beam to return to the top of the screen. *See* id. Hsync pulses also occur during the Vblank interval, which during the Vsync pulses are encoded as "serrations." *See* id. Hsync pulses (serrations) occur during the Vblank interval so that the beam will continue to scan horizontally even as it returns to the top of the screen. *See* id. The composite

sync signal, included within the composite television signal, includes both Hsync and Vsync pulses and is produced by a sync generator. *See* id. para. 17.

Lechner then describes the function of drive signals inside a television camera-to control the camera's scanning pattern. *See* id. para. 18. Lechner asserts that the sync signals sent to the television accomplish the same function in the television as the drive signals accomplish in the camera. *See* id. Thus, Lechner posits, the Hsync and Vsync signals contain drive signal information that controls the television scanning beam. *See* id.

As such, Lechner proffers a different definition of "drive signals" than Mayer. Lechner's definition is not limited to television cameras: "drive signals are known in the television electronics field to be signals that occur during the blanking intervals of a line and field respectively and control the timing of generating and displaying picture information." Id. para. 22. Lechner offers three prior patents in support of the proposition that "those working in the television electronics field referred to the Hsync and Vsync signals as drive signals." *See* id. para. 19 and Ex. C (the '390 patent), Ex. D (the '549 patent) and Ex. E (the '317 patent). Lechner insists that those patents refer to signals used by the television to control the television's deflection circuits as drive signals. *See* id. para. 19. Relyingon his definition of drive signals, Lechner testifies that a video tape recorder, despite not having its own scanning beam, incorporates drive signals. *See* id. para. 22.

In paragraphs 26-70 of his declaration, Lechner provides a detailed analysis of how the SNES incorporates the sync generator of the '659 patent. Lechner begins by testifying that both the '659 patent and the SNES create precision timing signals; Lechner refers to the SNES as a "miniature television studio." *See* id. para.para. 26-28.

After briefly reviewing the circuitry of the SNES, *see* id. para.para. 29-30, Lechner discusses how the SNES incorporates all of the elements of Claim 1 of the '659 patent. *See* id. para.para. 31-58.FN29 As to drive signals, Lechner testifies that the '659 patent "describes drive signals as being used to trigger the horizontal and vertical deflection circuitry of a television camera ... and further demonstrates that drive signals are used in the generation of the composite sync and [color] burst signals which are part of the television signal." Id. para. 44. Lechner avers that although the SNES does not produce the former drive signals, the SNES does produce the latter drive signals: "the SNES Hsync and Vsync signals contain the drive signal information to cause the horizontal and vertical deflection circuitry of the TV to begin the retrace process." Id. para. 48. Lechner also claims that the SNES produces other drive signals, including, *inter alia,* a vertical drive signal (the CSSEA 1 signal) used to create an interval analogous to the Vertical Drive Interval of the '659 patent. *See* id. para. 49; *see also* id. para. 50.

FN29. Although Lechner explains how the SNES incorporates each element of Claim 1, the Court will address Lechner's discussion only with respect to the two elements here at issue.

Lechner discusses the vertical counter element of Claim 1 in paragraphs 34-42. Lechner first reviews the advanced in phase signal of the '659 patent and states that the delay that that signal is designed to remedy would exist with either a synchronous or non-synchronous vertical counter. *See* id. para.para. 34-36.

Lechner then reviews the SNES circuitry and exclaims: "The HCLD pulse is the signal that increments the vertical counter. Just as in the '659 patent, the signal that clocks the vertical counter in the SNES is the signal that is being counted by the vertical counter." Id. para. 38. Furthering this viewpoint, Lechner states: "Since the HCLD signal reaches the vertical counter circuitry on horizontal count 338, prior to the highest horizontal count of 340 which corresponds to the lowest frequency signal produced by the horizontal counter, and since the HCLD signal increments the vertical counter, the HCLD signal clocks the vertical counter and is advanced in phase with respect to the lowest frequency signal produced by the horizontal

counter." Id. para. 39. Lechner posits that the SNES uses an advanced signal mechanism for the same reason as the '659 patent-to ensure that the vertical counter is incremented by the time the horizontal counter is reset to zero. *See* id. para.para. 40-41.FN30

FN30. In paragraphs 59-70, Lechner testifies as to how the SNES incorporates all of the elements of Claims 3, 4, 5 and 13 of the '659 patent. As the Court has stated above, Claim 1 incorporates all of the elements here at issue and is the only claim that is being addressed specifically. Thus, the Court does not here summarize Lechner's declaration with respect to Claims 3, 4, 5 and 13.

B. Discussion

1. Non-infringement of Claim 1 of the '659 Patent

[21] As indicated above, GE's allegation of infringement hinges on two elements of Claim 1 of the '659 patent. The central issues with respect to the elements at issue are (1) whether the term "drive signals" as claimed in the '659 patent is limited to signals produced by a television camera sync generator to control the deflection circuitry of the camera's electron scanning beam, and (2) whether the SNES incorporates a vertical counter that is clocked by a signal which is advanced in phase relative to the lowest frequency signal produced by the synchronous horizontal counter.

a. Literal Infringement

(1) Drive Signals

[22] Construction of the patent claim term "drive signals" is a matter of law exclusivelyfor the Court. *See* Markman v. Westview Instruments, Inc., 52 F.3d 967, 977 (Fed.Cir.1995), *aff'd,* 517 U.S. 370, 116 S.Ct. 1384, 134 L.Ed.2d 577 (1996). To ascertain the meaning of drive signals, the Court looks to the claim, the specification, the prosecution history and extrinsic evidence. *See* id. at 979. Based on the record before it, and for the reasons stated below, the Court concludes that "drive signals" means only those signals used inside a television camera to control the camera's deflection circuitry.

As to the claim, the language and context of Claim 1 provide little insight into the meaning of the term drive signals. Claim 1 merely requires that the sync generator being described generate "blanking, sync and drive signals." *See* Lechner Decl. Ex. B at col. 2, lines 56-57, 60-61 and 63-64. Yet, because the claim describes three separate types of signals, it is logical to conclude that each signal is distinct from the others.FN31 *Cf.* Ethicon Endo-Surgery v. U.S. Surgical Corp., 855 F.Supp. 1500, 1510 (S.D.Ohio 1994) ("When elements are specifically described in a claim as separate and distinct, it would be inconsistent to conclude that the author intended the one to be included in the other.").

FN31. That sync and drive signals are distinct is supported by the specification. *See* Lechner Decl. Ex. B at col. 6, lines 55-60 (describing separately the "COMPOSITE SYNC" signal and the "HORIZONTAL DRIVE/CHROMA" signal). The specification never describes sync and drive signals as overlapping or intertwined.

The specification, of which the claims are a part, generally discusses the use of sync generators in both television cameras and video tape recorders. *See* Lechner Decl. Ex. B, *id.* at col. 1, lines 9-16. It is undisputed that the latter does not have a need for drive signals in the definitional sense propounded by Nintendo. The specification, however, includes a specific definition of drive signals that is limited to television cameras only. *See id.* Ex. B at col. 6, lines 56-60 and col. 7, lines 44-46 (describing horizontal and vertical drive signals as those signals used to trigger the deflection circuitry inside a television camera).

The specification does not include any other definition of drive signals. As the Federal Circuit has often stated, a patentee is free to be his own lexicographer. *See* Markman, 52 F.3d at 980 (citing Autogiro Co. of Am. v. United States, 181 Ct.Cl. 55, 384 F.2d 391, 397 (1967)). The Court (and the public) may look to the patentee's own definition of claim terms to interpret the coverage of the claim. *See* In re Vogel, 422 F.2d 438, 441 (C.C.P.A.1970). The Court therefore views the definition of drive signals in the specification as strong evidence of the meaning of the term.

In an attempt to overcome its own patent language, GE argues that that "definition" is limited to the use of drive signals in the preferred embodiment and cannot be used to limit the claim. *See* GE's Br. in Opp. at 14. GE correctly asserts that "while it is true that claims are to be interpreted *in light of* the specification and with a view to ascertaining the invention, it does not follow that limitations from the specification may be read into the claims." *Id*. (quoting Sjolund v. Musland, 847 F.2d 1573, 1581 (Fed.Cir.1988) (emphasis in original)). The Court, however, does not here import a limitation into the claim that the patent did not itself include.

As conceded by GE, the public is entitled to rely upon the language of patent claims. *See id.;* Nintendo's Br. at 23-24 (citing Athletic Alternatives, Inc. v. Prince Mfg., Inc., 73 F.3d 1573, 1581 (Fed.Cir.1996) (a patent must particularly point out and distinctly claim the subject matter which the applicant regards as his invention)). Here, a reading of the claims in light of the specification leads to the unclouded conclusion that the subject matter of the '659 patent is television cameras and that the term "drive signals" is limited to those signals used to trigger the camera's deflection circuitry.FN32

FN32. The Court notes that extrinsic evidence in the record supports this conclusion. At the time the '659 patent application was filed, Dr. Marlowe's employer was RCA. In a document submitted to the Patent Office with respect to that application, one of RCA's in-house patent attorneys stated: "The subject matter [of the application] relates to television cameras." Blank Cert. Ex. 10 at 1.

In furtherance of its argument that the definition of drive signals in the specification is limited to the preferred embodiment, GE asserts that the term must be given its ordinary meaning. *See* GE's Br. in Opp. at 14. The parties dispute the ordinary meaning of "drive signals," and each submits extrinsic evidence-an expert certification and various exhibits-in an attempt to establish the ordinary meaning.

The Court finds that the ordinary meaning of "drive signals" refers to those signals generated to control a television camera's electron scanning beam. Thus, the ordinary meaning supports the Court's interpretation of the claim in light of the specification. Moreover, even if the specification was silent as to "drive signals," the Court would find in favor of Nintendo's proffered definition.

In so concluding, the Court finds the testimony of Nintendo's expert, Mayer, to be instructive. Mayer asserts that the traditional definition of drive signals was limited to signals used to control the camera's electron beam. In support, Mayer points to prior art relating to sync generators and drive signals, which describe drive signals as Nintendo claims. *See* Mayer Cert. para.para. 36-38 and Exs. E-G; *see also* id. para. 48. One of the texts quoted by Mayer was authored by an instructor at the RCA institute. *See* id. Ex. E. Also educative is the testimony of Dr. Marlowe, the inventor of the '659 patent who worked for RCA at the time the '659 patent was filed and issued. Dr. Marlowe testified that the traditional purpose of drive signals was to be used inside the camera only to control the camera's deflection circuitry. *See* Blank Cert. Ex. 3 at 187, lines 5-25.FN33 The prior art cited by Mayer coupled with Dr. Marlowe's testimony as to the traditional purpose of drive signals strongly supports the definition of drive signals set forth in the '659 patent specification.

FN33. Part of the cited portion of Dr. Marlowe's deposition transcript reads as follows:

Q (Counsel for Nintendo): So when you say in general terms, talking about the camera, the drive signals would be supplied to the deflection circuitry in the camera that causes the beam inside the camera to scan?

A (Dr. Marlowe): Yes. If the drive signals were used for their traditional purpose, that's where they would be applied. They would trigger, they would be applied to some other circuitry that would make the deflection happen.

The testimony of GE's expert, Lechner, does not alter the Court's conclusion. In support of his opinion that the traditional meaning of drive signals is broader than that stated by Nintendo, Lechner cites to three patents, which all purport to refer to drive signals as being used to control the deflection circuitry inside a television. *See* Lechner Decl. para. 19 and Exs. C-E. Lechner asserts that those patents show that certain sync signals actually contain drive information and, therefore, should be considered drive signals. *See* id. para.para. 18-19, 22.FN34

FN34. GE also cites to four publications, which exhibit the use of drive signals in test equipment for a television camera, special effects generators, pulse and bar generators, and window generators. *See* GE's Br. in Opp. at 19; Pollack Decl. Exs. B-E. For the reasons stated by Nintendo on reply, the Court finds these publications unpersuasive. *See* Nintendo Reply Br. at 6-7.

Lechner's testimony, however, attempts to overlap the respective definitions and functions of sync and drive signals. As the Court stated above, the claim language indicates that three distinct types of signals are generated by the '659 patent: blanking, sync and drive signals. Accepting Lechner's testimony would blur the otherwise clear lines separating the three types of signals.FN35 In light of the specification and Mayer's and Marlowe's testimony, the Court cannot conclude that Lechner's opinion of the meaning of "drive signals" is correct.

FN35. Indeed, the distinction between sync and drive signals is embodied in one of Lechner's own patents, United States Patent No. 4,709,256. In that patent, Figure 1 shows horizontal and vertical drive signals being sent from the sync generator to a television camera. Separate sync signals created by the sync generator are used to generate the composite video signal, which is sent to the television. *See* Nintendo's Reply Br. Ex. 1 at Figs. 1 and 2; col. 3, lines 33-36; col. 6, lines 34-42.

The Court therefore holds, as a matter of law, that "drive signals" as claimed by the '659 patent refers to only those signals that trigger the deflection circuitry inside a television camera. Accordingly, because the SNES indisputably has no electron scanning beam or need for drive signals as claimed by the '659 patent, the Court concludes that the SNES does not infringe the '659 patent; the SNES fails to generate drive signals as required by Claim 1 of the '659 patent.

(2) Vertical Counter Clocked by Signal Advanced in Phase

Claim 1 of the '659 patent requires, *inter alia,* that the vertical counter be clocked by a signal which is advanced in phase relative to the lowest frequency signal produced by the synchronous horizontal counter. *See* Lechner Ex. B at col. 18, lines 52-55. GE asserts that the SNES infringes Claim 1 because the SNES' HCLD signal is an advanced phase signal which clocks the SNES' vertical counter. *See* GE's Br. in Opp. at 23-29. The threshold issue underlying this allegation is whether the HCLD signal "clocks" the SNES' vertical counter. As discussed below, the Court finds that the HCLD signal does not clock the SNES' vertical counter; instead, the Court finds that the same system clock pulse that causes the horizontal counter to reset to zero also clocks the vertical counter. Thus, the signal that clocks the vertical counter in the SNES

is "in phase" with the lowest frequency signal produced by the horizontal counter-the signal produced when the horizontal counter resets to zero.

A counter's flip-flop can only be put into its next state when a signal at its clock input is received. *See* Mayer Cert. para. 27. Notably, Dr. Marlowe admitted that a flip-flop is "clocked" by a signal received at its clock input. *See* Blank Cert. Ex. 3 at 57, line 23 to 58, line 9; 59, lines 15-20; 71, line 4 to 72, line 2.

As set out above in section III.A.2.b, in the '659 patent, it is clear that the ADVANCE signal is an advanced phase signal that clocks the vertical counter. Although the ADVANCE signal has the same frequency as the lowest frequency signal produced by the horizontal counter in the '659 patent-the 2H signal-the ADVANCE signal is produced seven clock pulses before the 2H signal; the ADVANCE signal is therefore "advanced in phase" relative to the 2H signal. Because the ADVANCE signal is received by the vertical counter at its clock input and triggers the vertical counter to enter its next state, the ADVANCE signal "clocks" the vertical counter.

The HCLD signal in the SNES is indisputably not provided to the vertical counter's clock input; the HCLD signal is sent to special flip-flops in each of the PPUs, which special flip-flops, on the next system clock pulse, send a signal to the enable inputs of the vertical counters. In fact, because the vertical counter in the SNES is a synchronous counter, the only signal it receives at its clock input is that from the system clock; all counters in the SNES are synchronous and, therefore, receive system clock pulses simultaneously. GE does not claim that the system clock pulses received by the SNES vertical counter are advanced in phase.

Thus, the question is whether the HCLD, which is advanced in phase, "clocks" the vertical counter. The answer is no.

GE essentially argues that the HCLD signal clocks the vertical counter because it enables the vertical counter. This argument must be rejected. Instructively, Dr. Marlowe testified that supplying a signal to the enable input of a counter does not clock the counter. *See* id. at 73, lines 2-13. FN36 Dr. Marlowe's testimony appears consistent with the use of the term "clock" in the '659 patent and in the art, which recognizes a distinction between enable and clock inputs. *See, e.g.,* Mayer Cert. para. 67 and Ex. K. Indeed, a signal that is applied to an enable input, unlike a signal that is applied to a clock input, does not cause a counter to change states, but rather simply turns the counter on, so that it will begin counting clock pulses. *See* id. para. 32. Thus, the vertical counter in the SNES is not "clocked" by the HCLD signal received at its enable input.

FN36. The cited portion of Dr. Marlowe's deposition transcript provides as follows:

Q (Counsel for Nintendo): We have talked about a situation before where there is a synchronous counter which also, we don't want it to count every clock pulse so we inhibit it or have an enable input that enables it to clock when it receives that. When in such a situation where the-and the enable signal is received in advance of the clock pulse, okay? In such a situation would it be appropriate to say that the receipt by the enable input of the enable signal, would it be appropriate to say that that is clocking the counter?

A (Dr. Marlowe): Well, I would not say that.

Because the HCLD signal is the only signal that is advanced in phase in the SNES and because the HCLD signal does not clock the SNES' vertical counter, the Court holds that the SNES does not infringe Claim 1 of the '659 patent; the SNES does not have a vertical counter that is clocked by a signal which is advanced in phase relative to the lowest frequency signal produced by the horizontal counter.

b. Infringement Under the Doctrine of Equivalents

[23] On top of its allegation of literal infringement, GE contends that the SNES infringes Claim 1 of the '659 patent under the doctrine of equivalents. GE asserts that the SNES "produce[s] signals that operate in the same manner as drive signals inside a television camera; *i.e.*, to notify the picture gathering circuitry when the next line of horizontal picture information is to be collected." GE's Br. in Opp. at 30-31. GE also asserts that while the '659 patent discusses a non-synchronous counter, the claims do not require a non-synchronous counter; GE posits that non-synchronous counters and synchronous counters are interchangeable as vertical counters in the sync generator of the '659 patent. *See* id. at 31. For these reasons, GE argues that the SNES infringes Claim 1 of the '659 patent under the doctrine of equivalents.

The Court disagrees for several reasons. First, GE's argument ignores the fact that the sync generator claimed in the '659 patent was designed for a television camera, not a video game. Indeed, Dr. Marlowe testified that, although he was aware of an ongoing video game project at RCA, he never considered that the RCA video game would be an application for his sync generator. *See* Blank Cert. Ex. 3 at 36, line 25 to 37, line 11; 34, lines 4-8.

Second, the '659 patent uses drive signals to control the camera's scanning beam to capture real images. The SNES has no scanning beam and does not capture real images; the SNES creates computer-generated video game images. The signals used to create the images in the SNES necessarily perform fundamentally different functions, in fundamentally different ways to produce fundamentally different results than the drive signals claimed in the '659 patent.

Finally, as to equivalence of the vertical counters and the advanced in phase signal, the '659 patent uses an advanced in phase signal to address the propagation delay resulting from a non-synchronous vertical counter. This advanced in phase signal causes the vertical counter to begin changing state while the camera's electron beam is still scanning a horizontal line. By contrast, as stated in the patent specification, "[t]he use of a synchronous counter eliminates propagation delay problems which are inherent in non-synchronous counters." *See* Lechner Decl. Ex. B at col. 2, lines 16-19. The SNES uses a synchronous vertical counter, such that the vertical counters do not change state until after the beam has finished scanning a horizontal line. In fact, the vertical counter in the SNES is incremented at exactly the same time the horizontal counter is reset. The SNES requires this set-up because, unlike the '659 patent, the SNES' other circuits must be able to determine the state of the vertical counters while the beam is still scanning a horizontal line.

The construction and function of the SNES is therefore fundamentally different from the '659 patent. While GE contends that both synchronous and non-synchronous counters are interchangeable in the '659 patent because both exhibit propagation delay, the extent of the delay in the former is minimal. Indeed, Dr. Marlowe was unable to come up with any instance in which it would make sense to use a phase-advanced signal to clock a synchronous vertical counter. *See* Blank Cert. Ex. 3 at 100, line 5 to 103, line 10.

For all these reasons, the Court concludes that the SNES does not infringe Claim 1 of the '659 patent under the doctrine of equivalents. Because the Court has also found that the SNES does not literally infringe Claim 1, the Court will grant summary judgment of non-infringement in favor of Nintendo on Claim 1 of the '659 patent.

2. Non-infringement of Claims 3, 4, 5 and 13 of '659 Patent

As stated *supra,* Claim 3 is dependent upon Claim 1, and Claims 5 and 13 are dependent upon Claim 4. Claim 4 includes each of the elements of Claim 1 relevant to this litigation. Thus, because the Court has determined that Claim 1 has not been infringed literally or under the doctrine of equivalents, Claims 3, 4, 5 and 13 are also not infringed. The Court will include those claims within the grant of summary judgment of non-infringement in favor of Nintendo.

IV. UNITED STATES PATENT NO. 4,270,125

A. Background

United States Patent No. 4,270,125 (the " '125 patent"), entitled "Display System," was filed on September 13, 1976 and issued on May 26, 1981. *See* Mayer Cert. Ex. A (copy of '125 patent).FN37

FN37. GE includes a copy of the '125 patent as Exhibit B to the certifications of its experts, Robert Pelovitz and Joel Snyder.

1. Display Systems

The invention claimed in the '125 patent is a display system for retrieving picture information from the memory of a computer system in response to control signals from the computer. Display systems retrieve picture information and then convert that information into a video signal, which is combined with timing (or sync) signals generated in the display system to form a television signal. The display system at issue here retrieves picture information and maps the information onto a raster scanned display device. A raster is part of a display device, such as a television, that paints a picture on a screen by moving sequentially from left to right across a series of lines that combine to make up the picture.FN38 *See* Pelovitz Decl. para.para. 9-11. Thus, the circuitry of the '125 patented system, like display systems generally, provides a mechanism for taking information from a computer and displaying it as pictures on a television or other receiver.

FN38. See section III.A.1 for a discussion of how the picture is "painted" onto the television screen.

The basic components of a computer, which a display system incorporates, are: (1) a central processing unit (the "CPU"), which performs logic and arithmetic operations on data; (2) memory, which stores data; and (3) input/output systems, which receive data from or send data to devices, such as keyboards, displays, etc. Bundles of wires called "data busses" connect these components and allow data to be transferred among them. *See* Mayer Cert. para.para. 53-56.

There are two basic steps for creating a computer generated image on a television display. Step A involves loading into memory the data that will be processed and used to create an image on the television. Step B involves retrieving this data from memory and putting it into a form for transfer to the television, where it is used to display the desired picture on the screen. FN39 Step B is often referred to as "refreshing" the display. *See* Mayer Cert. para. 57.

FN39. The terms Step A and Step B are not industry accepted terms; rather, they are terms the Court has adopted from the certification of Nintendo's expert.

These two steps often involve distinct circuitry design considerations. Step A involves processing and storing data that will change from frame to frame and that will be used to show the motion of various objects, the changing of backgrounds, etc. Step B involves the constantly repeated transfer of information to the television with precise timing to provide the television's electron beam with information to allow it to "refresh" each part of the image at the appropriate time on the display screen sixty times each second. Step B requires large amounts of data to be transferred out of memory at precise times to provide necessary data in synchronization with the television's scanning electron beam. *See* id. para.para. 58-59.

There are generally two techniques for refreshing the display: (1) "bit mapping" and (2) "character generation." In the bit mapping technique, data for an entire screen is stored in memory such that each and

every spot on a television screen corresponds, on a one-to-one basis, to a specific location in memory. Each specific location in memory can be referred to as a display location, and there are the same number of display locations as there are spots to be displayed on a screen. *See* Mayer Cert. para. 85. Thus, an image appearing on a television screen corresponds in its entirety to picture information located in the bit map memory.

In a character generation system, small blocks or "stamps" of data representing portions of graphic images are stored in a memory called a "character data memory." A second memory, called a "character list memory," contains data specifying which stamps are to be used and the order in which they will be displayed to produce the desired image on the screen. *See* id. para.para. 91-93. The stamps in the character data memory remain the same, regardless of the image to be generated. The stamps can be repeatedly called up from memory and placed anywhere on the screen and do not have to be assembled in a memory before the image is created on the screen. Thus, unlike the bit mapping technique, there is no one-to-one correspondence between any display location and any spot on the television screen.

Character generation systems are particularly suited to the complex, fast action graphics required by video games because the images are assembled for the first time directly on the screen without using a full screen bit map memory. Further, character generation systems require less memory than a bit map system because character generation systems do not have memory locations for every spot on the screen as is required in a bit map system.

2. The '125 Patent

The '125 patent has two claims, both of which are independent. GE has asserted Claim 1 of the '125 patent against Nintendo's SNES and Gameboy video game systems.FN40 Claim 1 is written in "means-plus-function" format and provides as follows, with the bracketed letters included for reference:

FN40. GE had initially asserted Claim 1 against the NES, SNES and Gameboy systems and Claim 2 against the SNES system. GE, however, withdrew its allegation of infringement of Claim 1 against the NES system and its allegation of infringement of Claim 2 against the SNES system. "GE withdrew these allegations upon concluding, through analysis of certain documents produced by Nintendo in this case in the light of Nintendo's expert witness certifications and depositions of Nintendo's expert, that the NES does not include the eighth listed element of claim 1 ('gating means ... for coupling the output of the line counter means to the data bus means') and that the SNES does not include the eighth listed element of claim 2 ('an Exclusive-OR gate')." *See* GE's Br. in Opp. at 1 n. 1. Thus, only GE's allegation of infringement of Claim 1 against the SNES and Gameboy systems remains.

1. A system for displaying a pattern on a raster scanned display device by mapping bits from a display location in a memory associated with a computer onto the raster as contrasting spots depending on the value of each bit, wherein said computer is responsive to a direct memory access request to produce on a data bus, data signals retrieved from said memory at a location specified by a pointer address register, comprising the combination of:
[a] clock means for producing timing signals;

[b] output means for coupling signals to said display device;

[c] means, including interval timing means, responsive to said timing signals, for producing horizontal synchronizing signals and applying them to said output means;

[d] line counter means responsive to said horizontal synchronizing signals for producing output signals

identifying individual horizontal lines;

[e] first decoder means responsive to said interval timing means and to said line counter means for supplying direct memory access requests to said computer;

[f] second decoder means responsive to said line counter means for supplying vertical synchronization signals to said output means;

[g] means for storing data signals from said data bus in response to a signal derived from said timing signals when said computer responds to a direct memory access request and for shiftingsaid data serially to said output means in response to said timing signals; and

[h] a plurality of gating means, responsive to a command signal, for coupling the output signals from the line counter means to the data bus means.

Mayer Cert. Ex. A at col. 7, line 52 to col. 8, line 24.FN41
FN41. Claim 2 of the '125 patent is identical to Claim 1 except as in regards to the final element [h]. Element [h] of Claim 2 provides: "said output means including an Exclusive-OR gate receptive of said vertical and horizontal synchronizing signals for producing a composite synchronizing signal having horizontal serrations in said synchronization signal." Mayer Cert. Ex. A at col. 8, lines 56-60.

The claimed system consists of a circuit used to perform Step B-retrieving data from memory and putting it in a form for transfer to the television where it is used to refresh the display. The patent neither describes nor claims how Step A-the loading of data into memory-is performed. *See* id. para.para. 62-64.

The patent specification and its file history indicate that the circuit is simplistic and economical. The specification states: "A system embodying the invention comprises a relatively simple circuit which may be constructed from standard logic elements such as these [sic] commercially available in integrated circuit form...." Id. Ex. A at col. 1, lines 50-54. The file history states: "The important advantages of the present approach are its simplicity and relatively low cost." Bergin Cert. Ex. 2 at 55.

a. Data Transfer Technique

The preamble and elements [e] and [g] of the '125 patent refer to "direct memory access." These references relate to the method by which the '125 patent transfers data under Step B.

At the time the '125 patent application was filed, there were two or three well-known ways to carry out the data transfers involved in Steps A and B. FN42 The first, "CPU transfer," uses the CPU to transfer data in or out of memory. It is the slowest data transfer technique because the information must be transferred into and out of the CPU before being stored in memory or transferred to an input/output device. CPU transfer is also the least efficient technique because the CPU cannot perform other tasks (such as processing and generating new data) while it is transferring data. CPU transfer is, however, the least expensive data transfer technique. CPU transfer is often used for Step A, which generally involves the transfer of smaller and less time-critical amounts of data into memory. This technique, however, is not practical for Step B because, even for the simplest pictures, virtually all of the CPU's available time would have to be used to retrieve data from memory and transfer it to the television to refresh each display. *See* id. para. 60(a). Neither the '125 patent nor Nintendo's video game systems utilize the CPU transfer technique for Step B.

FN42. The Court states "two or three" because, as explained below, Nintendo asserts that there were three known methods, while GE argues that the third method is included in the second. This dispute is a central

issue with respect to the '125 patent litigation.

The second technique, "Direct Memory Access ('DMA') transfer," allows the transfer of data directly from memory, without moving the data into or out of the CPU. As discussed below, GE asserts that DMA transfer includes any transfer technique "by which data is transferred from one location in a computer system to another *without the intervention of the CPU*." *See* GE's Br. in Opp. at 9 (emphasis added). By contrast, Nintendo contends that under the DMA transfer technique, the DMA circuit shares the same data bus (data transfer wires) as the CPU, thus allowing only the DMA circuit *or* the CPU to operate at a given time. Because of this shared data bus configuration, Nintendo asserts, when the DMA circuit is used to perform Step B, the CPU is unable to be used for fifty percent of the time or more to perform other tasks.

Nintendo asserts that a third technique, "dedicated hardware transfer," allows the transfer of data without intervention of the CPU *or a sharing of the CPU data bus*. As described by Nintendo, a dedicated hardware display system contains its own dedicated display memory and its own data bus connections between that memory and the display system outputs. Under this configuration, transfer of data from the dedicated display memory to a display can be done independently of the CPU *and its data bus*. Consequently, the CPU can continue to process data even while the dedicated display hardware is transferring data to the television to refresh the display. This technique facilitates the transfer of large amounts of data very quickly, but because it requires additional hardware, it is the most expensive technique.

GE avers that because the dedicated hardware technique transfers data without the intervention of the CPU, it is nothing more than a variation of the DMA transfer technique. The '125 patent uses the DMA transfer technique to perform Step B and has no dedicated hardware.FN43 Due to the lack of dedicated hardware, the CPU cannot be used to perform other necessary tasks, such as Step A, while the DMA circuit is utilizing the shared data bus to perform Step B. This fact is acknowledged in the specification, which states "the processor time during display periods is necessarily devoted solely to display." Mayer Cert. Ex. A at col. 3, lines 58-60.

FN43. The '125 file history states: "The readout by direct memory access (DMA) is economical (no auxiliary memory is needed) [*i.e.*, the system has no dedicated hardware]." Bergin Cert. Ex. 2 at 49.

Thus, the '125 display system is limited in the complexity of images it can produce. As put forth by Nintendo and evidenced by the patent, the '125 patent system is "capable of displaying only very simple images. Under the '125 patent, each horizontal line consists of 64 black and white spots [or 'pixels'] (as compared with video game systems which even at that time [late 1970s] created 256 or more colored spots [pixels] per horizontal scan line). In addition, the '125 display system produces a display with only 128 horizontal lines (as compared with video game systems which produce displays consisting of 240 or more horizontal lines)." Nintendo Br. at 12 (citing Mayer Cert. Ex. A at col. 3, line 67 to col. 4, line 3).

b. Refresh Technique

The memory associated with the computer system described in the '125 patent stores picture information in the form of data bits in locations specified by memory addresses.FN44 When the memory is sent addresses corresponding to the data bits representing the picture to be displayed, the memory sends the data bits to an output circuit, called a "shift register," for every eight pixels on each line of the display screen. *See* Pelovitz Decl. para. 61. The shift register converts the data bits into a serial stream, which is then converted into a television signal representing the display of eight pixels of an individual line of picture information. This process is repeated over the entire television screen and is generally referred to as "refreshing" the image.

FN44. The data bits represent the screen image as contrasting light spots depending on the binary value of each bit. *See* Pelovitz Decl. para. 41.

The technique used in the '125 patent for refreshing the picture information is set forth in the preamble: "A system for displaying a pattern on a raster scanned display device by *mapping bits from a display location in a memory associated with a computer onto the raster as contrasting spots depending on the value of each bit*...." Mayer Cert. Ex. A at col. 5, lines 52-56 (emphasis added). The specification elaborates:

The video display is accomplished by mapping the memory bits devoted to the display onto a standard television raster. Each memory bit has a logical value of one or zero. Therefore, each bit can represent a light or dark spot at a particular location on the [television screen] depending on the bit's value.

Id. Ex. A at col. 2, lines 23-28; *see* id. Ex. A at col. 2, lines 29-48 (discussing how "each bit represent[s] a point on the raster" and how it is possible to "illuminate each spot on a given sweep line with a corresponding bit").

c. Gating Means

The final claim element relevant to this litigation is element [h] of Claim 1. Element [h] provides for "a plurality of gating means, responsive to a command signal, for coupling the output signals from the line counter means to the data bus means." Id. Ex. A at col. 8, lines 22-24. The referenced gating means is designed, at least in part, to deal with a problem caused by the crudeness of the images produced by the '125 display system. Because the '125 patent system only displays 64 spots on each horizontal line, the spots are not square, but instead are horizontally elongated. The '125 gating structure is designed, at least in part, to repeat the same picture data on several consecutive horizontal lines of the television screen so as to create greater vertical definition of the spots, thereby displaying squarer spots with less smear.

The structure of the '125 patent specification which corresponds to element [h] consists of five "gates" (which can be thought of as electronic devices which permit or stop the flow of a signal) connected between the "line counter" FN45 and a data bus, which transmits data to and from the microprocessor and its DMA circuit. The '125 line counter consists of eight stages (or flip-flops), which count values in binary format. These eight stages count values from 2^0 to 2^7 (*i.e.*, 0 to 255 in decimal format). *See* Mayer Cert. para.para. 21-23.

FN45. A line counter is a device which counts the number of horizontal lines which are displayed on a television screen. In the '659 patent discussion, *supra* section III, the line counter was referred to as the vertical counter.

The gates cause the system to repeat horizontal lines in the following way. As disclosed in figure 1 of the '125 patent, the gates are only connected to the five highest stages of the line counter (*i.e.*, the 2^3 to 2^7 stages). *See* id. Ex. A at fig. 1.FN46 These five highest stages, by themselves, count only in multiples of eight (*i.e.*, 8, 16, 24, etc.). The gates do not connect the lowest three stages of the line counter to the data bus. These lower three stages, which cyclically count from 0 to 7, are ignored. At the end of each horizontal line scan, a command signal activates the gates. When this occurs, the gates couple the values of the five highest stages to the data bus, and those values are then transferred by the CPU to the DMA circuit. Because the values of the upper stages change only once every eight counts of the line counter, the DMA circuit repeatedly transfers the same line of data to the television for eight consecutive horizontal lines. *See* id. Ex. A at col. 7, lines 4-15.FN47 The coupling of the gates to fewer than all of the line counter stages allows for this line repetition. If all eight stages of the line counter were connected by eight gates to the data

bus, different data would be transferred at the end of each horizontal line scan and there would be no line repetition at all. *See* id. para.para. 24-26.

FN46. Figure 1 of the '125 patent is attached as Appendix 4.

FN47. The '125 specification states that the plurality of gates in figure 1 repeats data for only two consecutive horizontal lines. *See* Mayer Cert. Ex. A at col. 7, line 4-6. Figure 1, however, shows the structure operating as discussed in the text above. Despite the discrepancy, the important aspect of the patent is that line repetition is achieved by connecting the gates to less than all of the stages of the line counter.

The result of this gating structure and the effect of line repetition is a display with low resolution. The '125 display system generates 128 horizontal lines on the display. The gating structure shown in figure 1 causes the same information to be repeated on eight horizontal lines. Thus, the display is left with only 16 horizontal bands (128 divided by 8) and can only show rudimentary objects. *See* id. para. 20.

3. Nintendo's Denial of Infringement

Nintendo's assertions concerning non-infringement of Claim 1 by its SNES and Gameboy systems are directed to three features of Claim 1, which Nintendo contends are absent in the SNES and Gameboy systems. The three features at issue are (1) the use of a "direct memory access" technique to retrieve the information to be displayed; (2) the refresh technique of "mapping bits" onto the raster; and (3) the "gating means" that are used to couple the line counter to the data bus.

a. Nintendo's SNES and Gameboy Systems

The SNES is a video game system that consists of various elements, including a console(in which lies the CPU and related display circuitry), a game cartridge and an RF switch. The SNES uses a television for a display device. FN48 To produce signals representing picture and timing information, the SNES CPU interacts with, among other things, its own memory, the game cartridge, and the dedicated hardware, including two Picture Processing Units ("PPUs") and Video Random Access Memory ("VRAM").

FN48. The Gameboy system uses a Liquid Crystal Display monitor, which is another form of raster scan device. *See* Pelovitz Decl. para. 9. Both parties appear to agree that "[t]his and other minor differences between the SNES and Gameboy circuitry do not affect the infringement analysis on this summary judgment motion." GE's Br. in Opp. at 12 n. 9; Nintendo's Br. at 25 n. 11. As a result, the Court will discuss specifically only the SNES, with the understanding that the discussion will apply equally to the Gameboy system.

The picture data is transmitted among the CPU, the PPUs and the VRAM through data busses. *See* id. para. 24. As in the circuitry of the '125 patent, before the SNES can display a picture, the game program must first perform Step A; it must load picture information into the display memory-in the SNES, this includes the VRAM. Once loaded, the SNES data transfer process can retrieve the picture information from the VRAM by specifying an address that corresponds to a memory storage location. This is the first stage of Step B.

Unlike the '125 patent, the SNES' CPU data bus is not used in carrying out Step B. Instead, in the SNES, the dedicated hardware PPUs are the only devices capable of retrieving data from the dedicated display memories, including the VRAM, and transferring that data directly to the shift registers for display on the

screen. *See* Mayer Cert. para. 73-75, 77. Indeed, while the SNES has DMA circuitry similar to that in the '125 patent, that circuitry is used to perform only Step A; the design of the SNES system precludes that circuitry from performing Step B. In fact, the SNES' DMA circuitry FN49 has no direct connection to the shift registers, to which picture information is sent just prior to display on the television. *See* id. para. 76. Thus, the SNES' dedicated hardware circuitry performs Step B independently of the CPU, the SNES' DMA circuitry and the memory associated with the CPU. Due to this configuration, while the dedicated hardware is producing the display, the SNES' CPU can be performing other tasks, such as reading and processing instructions in the game program contained in the game cartridge, reading and processing information received from the game controllers being used by players, and generating new data to be transferred into the system memories. *See* id. para. 77. During display, however, the CPU does not have access to the dedicated display memories; thus, the CPU cannot load additional picture information into those memories (Step A) while the dedicated hardware transfers picture information from memory to display (Step B). *See* Lewis Decl. Ex. A at 832, lines 8-25; Pelovitz Decl. para. 70.

FN49. By reference here to the SNES' DMA circuitry, the Court refers to the DMA circuitry internal to the SNES that utilizes the CPU data bus. This circuitry is distinct from the SNES' Step B circuitry, which operates independently from the CPU data bus.

Nintendo included dedicated hardware in its video game systems so as to be able to create complex, high resolution video game images that would be commercially successful. *See* Nintendo Br. at 26. The '125 patent design is limited in its ability to create detailed images, in part, because the CPU generally is rendered inoperative during Step B. By contrast, the SNES' dedicated hardware allows the CPU to continue to perform during Step B. In fact, the use of dedicated hardware permits the CPU to use over 95% of its available time to perform functions essential to the generation of the complex images in Nintendo's video games. *See* Mayer Cert. para.para. 81-82.

As to the refresh technique, the SNES uses a character generation system. Thus, in the SNES, to create different images on the screen, the PPUs select character stamps from the character data memory in accordance with instructions in the character list memory. The stamps are then arranged on the screen to create a mosaic picture, and the picture is reconstructed and refreshed frame by frame. The SNES does not use a bit mapping technique.

Finally, as to gating means, the SNES, like the '125 patent, has a structure which allows the CPU to read the values of the line counter; the line counter is coupled to the data bus. Unlike in the '125 patent, however, in the SNES, *all* of the stages of the line counter are coupled to the data bus. The SNES' CPU can therefore determine at any time the precise horizontal line then being displayed. The SNES does not incorporate any arrangement to couple only a portion of the line counter to a data bus. Thus, the structure of the SNES cannot be used to repeat the same picture data on multiple horizontal lines.

b. Nintendo's Arguments in Support of Non-Infringement Claim

In support of its non-infringement claim, Nintendo argues that (1) the SNES uses a dedicated hardware technique to transfer data under Step B, which is fundamentally different from the DMA data transfer technique used in the '125 patent; (2) the '125 patent requires the use of a bit mapping display system, which is different from the character generation display system used in the SNES; and (3) the SNES does not use "a plurality of gating means" as required by element [h] of Claim 1.

(1) Data Transfer Technique

Nintendo asserts that the references to DMA in the preamble and elements [e] and [g] of the '125 patent,

coupled with the corresponding structure in the patent specification, requires a conventional DMA circuit. Nintendo reminds that because Claim 1 is written in means-plus-function format, it must be construed to cover only the corresponding structure disclosed in the '125 patent specification and equivalents thereof. *See* 35 U.S.C. s. 112(6). FN50 Nintendo insists that "the disclosed structure of the DMA circuit, the CPU, the data bus of the '125 patent, and their interconnection circuitry are necessarily part of the 'corresponding structure' under Section 112(6)." Nintendo's Reply Br. at 7.

FN50. Nintendo argues that the references to DMA in elements [e] and [g] must be construed, in light of the specification, as requiring DMA circuitry for carrying out Step B. The specification states that "[t]he computer has facilities for direct memory access to read memory data from a location specified by a pointer register onto a data bus." Mayer Cert. Ex. A at col. 1, lines 57-59.

Nintendo then avers that this structure discloses a conventional DMA circuit, which Nintendo describes as one that transfers data *over the CPU data bus*. *See* Nintendo's Br. at 25-26; Nintendo's Reply Br. at 8.FN51 Nintendo contends that GE improperly defines "direct memory access" to include any data transfer that does not involve the CPU, regardless of the use of the CPU data bus. Utilizing its definition of DMA, Nintendo insists that its dedicated hardware circuitry is fundamentally different from the '125 circuitry because it does not use the CPU data bus during Step B.

FN51. Nintendo also asserts that a conventional DMA circuit is used to perform Step A. *See* Nintendo's Reply Br. at 5.

Nintendo avers, and GE does not deny, that during Step B the '125 DMA circuitry utilizes the same data bus as the CPU; thus, the CPU generally is rendered inoperable while the DMA circuitry is utilizing the CPU's data bus to refresh the screen (*i.e.*, perform Step B). As noted in the specification, "the processor time during display periods is necessarily devoted solely to display." Mayer Cert. Ex. A at col. 3, lines 58-60. Nintendo asserts that this problem resulting from the shared data bus is characteristic of a conventional DMA process. In support, Nintendo points out that in a 1978 article co-authored by the inventor of the '125 patent, Joseph Weisbecker ("Weisbecker"), he recognized this characteristic of DMA circuitry in the context of refreshing a color display:

[D]uring refresh, the contents of the refresh memory have to be transferred to the external circuitry through a direct memory access (DMA) facility. The large amount of data to be transferred in this approach will strain or even breakdown the DMA process and *leave little or no processing time to the CPU*.

Mayer Cert. para. 60(b) and Ex. D at 137.

By contrast to the '125 patent, the PPU dedicated hardware that performs Step B in the SNES operates independently of the CPU and its data bus. Indeed, the SNES DMA circuitry used to perform Step A is not even connected to the shift registers, to which video information is sent and stored during Step B. Consequently, during display, the SNES' CPU remains available to perform other tasks. Nintendo asserts that the structure of the SNES circuitry is vital to the production of complex, video images and that if the SNES used the DMA circuitry as configured in the '125 patent, the SNES would be unable to generate the high quality graphics necessary for commercially successful video games.

Nintendo insists that: "No person reading this patent could reasonably believe that it was not limited to a conventional DMA structure, and, instead, covered all devices that transferred data from one point to another without the use of a microprocessor." Nintendo's Reply Br. at 7. Thus, "[a] properly instructed jury could not conclude that Nintendo's dedicated hardware is 'an insubstantial change which adds nothing of

significance to the structure ... disclosed in the patent specification." Nintendo's Br. at 27 (quoting Valmont Indus., Inc. v. Reinke Mfg. Co. Inc., 983 F.2d 1039, 1041-43 (Fed.Cir.1993)).

(2) Refresh Technique

Nintendo argues that its character generation refresh technique is fundamentally different from the bit mapping technique allegedly required by the '125 patent. In support, Nintendo emphasizes the differences between the two techniques, as set out *supra* section IV.A.1. Nintendo also cites to an article by Weisbecker, in which Weisbecker acknowledged these differences:

The discussions above point out some of the design tradeoffs associated with different display approaches. The memory mapped approach [bit mapping] requires relatively simple hardware but extensive memory and software processing, whereas in the block or object approach [character generation], memory is saved by using more complex hardware. As described earlier, in the object oriented display, the objects are moved by simply changing the display addresses. The major portion of the processing is delegated to the hardware. Thus, the motion can be very fast. In the memory mapped approach, however, moving one pattern from one location to another involves considerable software processing on the refresh memory. It takes time and can be slow. Hence, the memory mapped approach puts restrictions on implementing fast, action oriented games.

Mayer Cert. Ex. D at 136. Nintendo also points out that these differences were recognized by RCA, the original assignee of the patent, during the prosecution of the patent. *See* Nintendo's Br. at 30 (citing Bergin Cert. Ex. 2 at 54-55).

To give significance to these differences, Nintendo strenuously argues that the '125 patent requires a bit mapping system. *See* Nintendo's Reply Br. at 9-11. Nintendo contends that "the preamble as well as elements [e] and [g] of Claims 1 and 2 require the use of the DMA screen refresh technique in the context of a bit map display system." Nintendo's Br. at 27. While Claim 1 does not specifically use the term "bit mapping," Nintendo opines that the use of the phrase "mapping bits" in the preamble, coupled with the disclosed structure corresponding to the means clauses and language from columns two and three of the specification, limits the claim to a bit map system. *See* Nintendo's Reply Br. at 9-11. Nintendo insists that the preamble is made part of the claim because it is incorporated by reference throughout the body of the claim. *See* id. at 10-11 (citing Bell Communications Research, Inc. v. Vitalink Communications Corp., 55 F.3d 615, 621 (Fed.Cir.1995)). Nintendo also asserts that because Claim 1 is written in means-plus-function format, the elements must be construed to cover only the disclosed structure and equivalents thereof. *See id.* at 11 (citing 35 U.S.C. s. 112(6)). Nintendo concludes that "[w]hen Section 112(6) is properly applied to the '125 patent, and the corresponding structure is considered, it is clear that Nintendo's character generation system is far removed from the '125 patent that utilizes a specific DMA circuit to transfer data from a full screen bit-map to the screen of a television...." Id. at 11.

(3) Gating Means

The last element of Claim 1 requires a "plurality of gating means." Nintendo again states that because this element is written in means-plus-function format, it must be construed to cover only the disclosed structure and equivalents thereof. *See* Nintendo's Br. at 20; Nintendo's Reply Br. at 2-3 (quoting Pennwalt Corp. v. Durand-Wayland, Inc., 833 F.2d 931, 934 (Fed.Cir.1987), *cert. denied,* 485 U.S. 961, 108 S.Ct. 1226, 99 L.Ed.2d 426 (1988)). Nintendo asserts that the structure corresponding to this claim element is the arrangement of gates which are coupled between the data bus and the five highest stages of the line counter. Referring to the specification, Nintendo avers that the only purpose of this structure disclosed in the patent is line repetition. *See id.* Nintendo also states that any other purpose of the gating structure asserted by GE is "frivolous." *See* Nintendo's Reply Br. at 3.

Nintendo contends that, although the SNES has a structure that couples the line counter to the data bus, the SNES does not contain any gates or other structure that couples only a portion of the line counter to a data bus. *See* Nintendo's Br. at 21. Thus, Nintendo insists, the SNES has no ability to repeat data on multiple horizontal lines and has a fundamentally different structure than the '125 patent. *See* id.; Nintendo's Reply Br. at 4.

Nintendo also points out that the SNES is designed to read the value of its line counter at any time, whereas the '125 patent is designed to read the value of its line counter only at the end of a horizontal line. *See* id.

4. GE's Reply to Nintendo's Non-Infringement Analysis

GE argues that Nintendo's non-infringement analysis is erroneous because: (1) the '125 patent does not require a specific DMA circuitry and, therefore, is not limited to circuitry that utilizes the CPU data bus; (2) Claim 1 of the '125 patent does not require a bit mapping refresh technique; and (3) the SNES includes the gating means required by element [h] of Claim 1.

a. Data Transfer Technique

In contesting Nintendo's assertion that its dedicated hardware circuitry is fundamentally different from the DMA circuitry required by the '125 patent, GE first argues that the DMA transfer process referred to by the '125 patent does not require any specific type of circuitry. *See* GE's Br. in Opp. at 27. Rather, GE posits, the '125 patent covers any circuitry that performs the data transfer claimed in elements [e] and [g].

At the heart of GE's argument is the premise that Nintendo has technically misconstrued the means-plus-function elements of Claim 1. GE disputes Nintendo's assertion that elements [e] and [g] "require a specific DMA structure" to perform Step B. Id. at 25 (quoting Nintendo's Br. at 25). Instead, GE asserts that the plain language of element [e] requires only a decoder means for supplying a DMA request to the computer. As to the "DMA request" language in element [e], GE contends that it is part of the function only. Thus, GE posits, "Nintendo is wrong when it asserts that the DMA process and circuitry is part of the 'means' portion of this claim element." Id. As to element [g], GE asserts that the plain language requires only means for storing and shifting data. GE explains that "[a]lthough the data that is stored and shifted is retrieved in response to a DMA request, the DMA process and circuitry is not part of the means or the function of this claim element." Id. Because of the above, GE maintains that while s. 112(6) is applicable to elements [e] and [g], resort to the specification is necessary *only* to ascertain the structure (and equivalents) corresponding to the "first decoder means" of element [e] and the "means for storing ... and for shifting" of element [g]. GE avers that the SNES includes identical or equivalent structure for performing the functions specified in elements [e] and [g]. *See id*. at 26.

GE further argues that the SNES performs Step B through a DMA process. GE avers that the SNES transfers data without intervention of the CPU, which GE insists "is the commonly understood definition of DMA." *Id*.FN52That the SNES CPU can performother functions and that Nintendo labels its circuit "dedicated hardware," GE asserts, are irrelevant. *See id*. at 27 n. 15. GE therefore concludes that, like the '125 patent, the SNES uses a DMA process.

FN52. GE also maintains that Nintendo's use of a DMA data transfer technique is confirmed by the fact that the SNES's CPU is unable to access the dedicated display memory during Step B. *See* id. at 26-27.

GE's argument on this issue is concise and reads, in relevant part, as follows:

The circuitry that performs the DMA process is sometimes called "dedicated hardware," because this generic term refers to circuitry that performs specific functions in a computer system. Thus, Nintendo's asserted distinction between DMA and so-called "dedicated hardware" transfer is also erroneous. Irrespective of the specific circuitry used, transferring data from one location in a computer system to another without the intervention of the CPU is a DMA transfer process. This is all claim 1 requires and it is plainly found in the accused Nintendo products.

In the SNES and Gameboy systems, the output signals from the horizontal and vertical counters are decoded, resulting in signals that correspond to the active display interval. These signals initiate the process of transferring data from VRAM to the display screen without intervention of the CPU. (Pelovitz Decl. para.para. 58, 77.) Thus, these signals are direct memory access requests from the first decoder means, as per the fifth listed element of claim 1. (Id.)

When the SNES or Gameboy computer responds to these DMA requests, the data is temporarily stored in shift registers which shift that data serially to the output means and, ultimately, to the display screen. (Pelovitz Decl. para.para. 62, 79.) Thus, the last portion of the seventh listed element of claim 1 is also met by these Nintendo products. Therefore, Nintendo's second non-infringement assertion must also fail.

Id. at 27-28 and n. 16 (citing to Lewis Decl. Exs. B and C-two United States patents that purport to refer to DMA circuitry as dedicated hardware).

b. Refresh Technique

Nintendo's argument that the '125 patent requires a bit map display system is rooted in the preamble of Claim 1, which describes the claimed invention as: "A system for displaying a pattern on a raster scanned display device *by mapping bits from a display location in a memory associated with a computer onto the raster as contrasting spots depending on the value of each bit*...." Mayer Cert. Ex. A at col. 7, lines 52-56. GE, however, argues that the preamble cannot be used to limit the claims because the claims completely define the subject matter. GE avers that each element of Claim 1 defines the invention without regard to how data is stored in memory. Thus, GE concludes, the preamble is not necessary to properly define the invention, and the preamble, including the "mapping bits" language, is not a claim limitation. *See* GE's Br. in Opp. at 29-30.

Moreover, GE argues that even if the preamble were considered, the "mapping bits" language does not limit the claim; rather, that language "merely specifies that the invention is intended to be used with raster scan displays." Id. at 30. GE explains that "[a]ll raster scan displays receive video information in pixel-by-pixel (or bit-by-bit) format. Therefore, a display system for a raster scanned screen must necessarily "map bits" onto the raster." Id. GE contends that because the SNES displays information on a raster scanned device, it also "maps bits." *See* id. at 30-31 ("Although [the SNES character generation system] stores data in cells and displays a picture containing characters, the picture data is mapped onto the display in bits."). GE also asserts that the SNES stores picture information in cells, each of which consists of a bit-mapped image. *See* id. at 31. Thus, GE argues, because the SNES displays and stores picture information in bit-mapped format, the SNES meets the "mapping bits" preamble language.

Further, GE maintains that "even if Nintendo were able to import a *complete screen* bit map memory limitation into claim 1, the fact question of infringement under the doctrineof equivalents would remain. The techniques of storing picture data in a complete screen bit map and/or smaller cells representing portions of characters were both known to the art at least as early as the 1970's ... as interchangeable methods of displaying stored information." Id.

Finally, GE states that Nintendo's attempt to characterize a statement in the '125 file history as an admission

of a bit map system is unavailing. *See* id. at 32-33. In that statement, the '125 patent attorney distinguished the '125 patent from a referenced patent, which utilized a character generation system, by pointing out that the latter cannot display "any desired configuration of dots." *See* Bergin Cert. Ex. 2 at 46. Nintendo argues that the quoted statement constitutes an admission that the '125 patent claims a complete screen bit map. GE declares that it does not, stating only that the term "bit mapping" is not mentioned anywhere in the patent or in the file history and that the statement is taken out of context. *See* GE's Br. in Opp. at 32-33.

c. Gating Means

Nintendo argues that the SNES does not have "a plurality of gates, or anything equivalent thereto, that couples *only a portion of* the line counter onto a data bus for any purpose, let alone *to repeat the same information on consecutive horizontal lines of the display*." Nintendo's Br. at 21 (emphasis added). GE responds that "the claim itself says nothing about coupling 'only a portion of' the line counter to the data bus[, n]or does the claim specify, as the function of the 'gating means,' repeating information on consecutive horizontal lines." GE's Br. in Opp. at 21.

GE asserts that the function stated in element [h] is "coupling the output signal from the line counter means to the data bus means," and GE contends that no additional functions (*i.e.,* line repetition) should be added to claim element [h]. *See* id. at 21, 23 (citing Transmatic, Inc. v. Gulton Indus., Inc., 53 F.3d 1270, 1278 (Fed.Cir.1995)).

As to the SNES, GE states that the output signals from the line counter are coupled to the data bus. Thus, GE declares, the SNES performs the function stated in the claim. GE then proceeds to explain how the means in the SNES, "tri-state buffers," are equivalent to the corresponding structure in the '125 patent, "AND gates." FN53 *See* id. at 23-24.

FN53. Nintendo does not contest that its tri-state buffers are equivalent in operation to GE's AND gates. Nintendo, however, argues that the issue is not the device used to transfer the output signals, but, rather, the structure of how the line counter is coupled to the data bus. *See* Nintendo's Reply Br. at 4-5.

5. Expert Testimony FN54

FN54. As with the parties' briefs, the Court summarizes only those portions of the expert testimony that are relevant to issues remaining in this case.

a. Steven Mayer for Nintendo

Mayer's background is briefly set out in section III.A.5.a above. With respect to the '125 patent litigation, Mayer has studied (1) the '125 patent, (2) its prosecution history, including the prior art references, (3) relevant sections of the SNES and Gameboy manuals and relevant sections of the logic level schematics of their CPU and PPUs, (4) a number of prior art documents that were not before the Patent Office, and (5) certain documents produced by GE and third parties to Nintendo.

Mayer concludes that the SNES and Gameboy systems do not infringe Claim 1 of the '125 patent because they: (1) do not use, as required by elements [e] and [g] of Claim 1, DMA circuitry to transfer data from a memory directly to a television for display; (2) do not have, as required by Claim 1, a structure for mapping bits from a display location in a memory onto a television; and (3) do not include the plurality of gating means required by element [h] of Claim 1.

In paragraphs 53-72, Mayer discusses some general principles of computer systems and the display system

claimed in the '125 patent. Here, Mayer introduces Step A and Step B and the different techniques for transferring data. *See supra* s. IV.A.1. Notably, Mayer distinguishes between the DMA technique and the dedicated hardware technique. *See* Mayer Cert. para. 60. In distinguishing the two techniques, Mayer quotes an article written by an RCA engineer in the 1970s, which recognizes the difference between DMA transfer and dedicated hardware transfer:

Refresh-Display refresh is required because of the dynamic storage characteristic of the CRT [the tube in the television]. There are two popular techniques for display refresh, DMA and dedicated-hardware controlled.

Id. para. 61 and Ex. C at 18.

Mayer then explains that because the '125 patent's DMA circuitry utilizes the CPU data bus to transfer data directly to the television for display, the circuitry generally renders the CPU inoperable during Step B data transfers:

[T]he '125 CPU cannot be used while the DMA circuit is performing Step B in order to refresh the display.... In other words, while the DMA circuit is being used to refresh the display, the '125 system's CPU cannot be used to perform other necessary tasks, including Step A.

Id. para. 67. Mayer posits that the preamble and elements [e] and [g] of Claim 1 embody the DMA circuitry requirement. *See* id. para. 70.

In paragraphs 73-83, Mayer discusses his conclusion that the SNES and Gameboy do not use the DMA technique to transfer data during Step B. Mayer centers his conclusion on the premise that the SNES uses a dedicated hardware technique, which is distinct from the DMA technique claimed in the '125 patent. The crucial difference between the '125 DMA technique and Nintendo's dedicated hardware technique is that, unlike the former, the latter "performs the Step B of transferring data to the display independently of the CPU, the DMA circuit and memory associated with the CPU. Thus, while the dedicated hardware is producing the display, the CPU can be performing other tasks...." Id. para. 77. Mayer teaches, that although the SNES and Gameboy have DMA circuitry, that circuitry is used only to perform Step A and is not even directly connected to the shift registers, where information is sent and stored during Step B just prior to being sent to the television for display. *See* id. para.para. 76 and 78.

Mayer explains that Nintendo's video game systems require the dedicated hardware technique so as to produce complex, high resolution video images that otherwise would be impossible to produce using the '125 DMA circuitry. *See* id. para. 81. Indeed, Mayer testifies, use of the more efficient and capable, albeit more expensive, dedicated hardware technique was a decision made by Nintendo to create commercially successful video games. *See* id. para. 80.

In paragraphs 84-103 of his certification, Mayer discusses his conclusion that the '125 patent claims a bit mapped display system, which is lacking in Nintendo's video games. Mayer first explains the difference between a bit mapped system and a character generation system. *See* id. para.para. 84-86, 90-94; *supra* s. IV.A.1.

Mayer then asserts that the '125 patent requires a bit map display as follows:

The requirement of using a bit map display is set forth in the preamble of claims 1 and 2. The bit map requirement is also present in elements [e] an [g] of claims 1 and 2, which require the DMA circuit to retrieve data from the memory and transfer it directly to the video shift register. These claim elements are written in means-plus-function format. As described above, these claim elements must be construed to

cover the corresponding structure disclosed in the specification and equivalents of that structure. The corresponding structure in the '125 patent specification includes a bit map memory which includes a storage location for each spot on the television display.

Mayer Cert. para. 89.

Mayer contends that this claim construction is supported by both the patent specification and the file history. As to the former, Mayer quotes the description of the display system found in the '125 specification:

The video display is accomplished by mapping the memory bits devoted to the display onto a standard television raster. Each memory bit has a logical value of one or zero. Therefore, each bit can represent a light or dark spot at a particular location on the [television screen] depending on the bit's value.

See id. para. 87 (quoting id. Ex. A at col. 2, lines 23-28). As to the latter, Mayer quotes a portion of the file history where RCA explained to the Patent Office the distinction between the bit mapped system allegedly claimed by the '125 patent and the character generation system found in a prior art reference:

The important differences in structure between the claimed invention and the reference as pointed out above result from the differences of purpose and operation of the two systems.... [The reference's] system reads a character from memory in the form of binary digits, decodes the character into a matrix of dot elements, and then displays the dot matrix to provide the configuration of the character. The circuit of [the reference] patent is thereby restricted only to characters which are coded into stored binary values and capable of being generated by the character generator, whereas the system of the invention can display any desired configuration of dots.

See id. para. 90 (quoting Bergin Cert. Ex. 2 at 54-55).

Mayer then discusses the use of the character generation system in Nintendo's video games and concludes that "Nintendo's character generation display system is substantially different from the bit map display required by the claims of the '125 patent." *See* id. para.para. 100-102.

In paragraphs 19-31 of his certification, Mayer explains the reasons for his conclusion that the SNES and Gameboy do not contain element [h] of Claim 1. Mayer first describes the structure of the '125 patent corresponding to the "plurality of gating means." In those paragraphs, Mayer discusses how the gating structure of the '125 patent allows for line repetition so as to improve the crude picture produced by the '125 patent's display system. FN55 Notably, Mayer testifies that " '125 patent discloses a specific structure for vertically repeating the same information on eight consecutive lines ... [and that the] only reason the gate structure was included in the '125 display system was to cause the same data to be repeated on successive horizontal lines, to partially compensate for the crudeness of the picture produced by the '125 display system. This structure has no other purpose." Id. para.para. 20-21.

FN55. Much of Mayer's discussion overlaps the discussion in section IV.A.2.c above and will not be summarized.

Mayer opines that because element [h] is written in means-plus-function format, that element is limited to the corresponding structure disclosed in the patent specification. *See* id. para. 27. As shown in figure 1 of the '125 patent, Mayer discusses how the gates disclosed in the '125 patent specification are only connected to the five highest stages of the line counter. *See* id. para. 24; App. 4 (gates designated as "110"). Mayer explains that in order to repeat lines, the gates in the '125 patent cannot be connected to all of the stages of the line counter. Indeed, "if all eight stages of the line counter in the '125 patent were connected by eight

gates to the data bus, there would be no line repetition at all, which would negate the purpose of those gates." Meyer Cert. para. 26.

Mayer then addresses the SNES and Gameboy and concedes that they have a structure that allows the CPU to read values of the line counter. Yet, Mayer declares,

unlike the gate structure in the '125 patent, which omits reading lower stages of the line counter, in the Gameboy and SNES systems *all* of the values of the line counter are coupled to the data bus. This structure cannot practically be used to repeat lines. Instead, in Gameboy and the SNES, the CPU uses this information to determine the horizontal line currently being displayed. The Gameboy and SNES systems use this information to accomplish certain tasks including creating effects such as scrolling the image on the display from right to left. For this feature to work, however, it is necessary for *all* of the line counter values to be coupled to the CPU's data bus. Neither Gameboy nor the SNES contains gates or any other structure that can couple only a portion of the line counter to a data bus for any purpose at all, let alone to repeat lines on the display screen.

Id. para. 29.

b. Robert Pelovitz for GE

Robert Pelovitz ("Pelovitz") has been an engineer working in the field of electronics related to computer display systems for nearly 15 years. His experience in this field is primarily the result of his responsibilities as an engineer at Sanders Associates Inc. between 1982 and 1996. Pelovitz has been retained by GE. *See* Pelovitz Decl. para.para. 1-3.

Pelovitz has examined (1) the '125 patent, (2) its file history, (3) the SNES and Gameboy, and (4) various documents produced by Nintendo to GE. Pelovitz concludes that the SNES and Gameboy systems incorporate all of the elements of Claim 1 of the '125 patent. In particular, Pelovitz asserts that the SNES and Gameboy infringe the '125 patent because they: (1) use a DMA process to transfer data during Step B; (2) map bits representing picture information onto a raster scan display device; and (3) use gating elements to couple a display line counter to a computer data bus. *See* id. para. 4.

In paragraphs 6-22 of his declaration, Pelovitz discusses computer display systems generally and the structure of the '125 patent specifically. Much, if not all, of this information has been set out above. Notably, however, Pelovitz describes only two techniques for transferring data-CPU transfer and DMA transfer. *See* id. para.para. 12-13. Pelovitz asserts that the '125 patent utilizes DMA transfer, using the CPU data bus, but without intervention of the CPU. *See* id. para. 18. In paragraphs 6-22, Pelovitz offers no explanation of the technique used by the '125 patent to refresh the image. As to "gating means," however, Pelovitz testifies that the '125 gating structure "allows the computer to use the line count value in a *variety of ways,* [one of which is to] display[ ] the same picture data on several adjacent lines." Id. para.para. 21-22 (emphasis added).

In paragraphs 23-39 of his declaration, Pelovitz describes the operation of the circuitry in the SNES. As to the data transfer technique used in the SNES, Pelovitz avers:

During the active display interval, the SNES reads the data out of the VRAM in a bit form organized to correspond to the display lines on a TV. Since the SNES transfers bits of picture data from the VRAM to the picture data shift registers *without the intervention of the CPU* during the active display interval, the SNES performs a DMA process in retrieving this display data.

Id. para. 33 (emphasis added); *see* id. para. 34.

As to how pictures are created by the SNES, Pelovitz states that the SNES stores picture information in picture cells in "bit form." Id. para. 25. Pelovitz asserts that the "cell numbers are stored in the VRAM as a map corresponding to the physical location of the picture cell on the TV display. This map is at least as large as the TV display area." Id. Pelovitz also avers that the SNES creates "each of its pictures from a group of picture cells, indexed by cell number, that are mapped onto the TV." Id. para.para. 25-26. Pelovitz emphasizes that the "SNES can display any desired configuration of light spots to develop TV pictures" by either drawing on the VRAM for pre-loaded picture cells or by creating additional picture cells. Id. para. 27.

Finally, Pelovitz discusses the coupling of the SNES's vertical line counter and a data bus. *See* id. para.para. 28-32.

In paragraphs 40-65 of his declaration, Pelovitz meticulously discusses how the SNES incorporates each of the eight elements of Claim 1.FN56 In this portion of his declaration, Pelovitz reasserts that the SNES utilizes a DMA data transfer technique. *See* id. para. 46.

FN56. In these paragraphs, Pelovitz technically analyzes each of the claim elements and compares them to the SNES. During the discussion, Pelovitz focusses on the claim language and makes scarce reference to the '125 patent specification. Pelovitz similarly analyzes the Gameboy system at paragraphs 66-81.

Pelovitz also addresses the "mapping bits" language in the preamble of Claim 1 and describes a purported similarity between the refresh techniques used in the '125 patent and the SNES. Pelovitz asserts that the system claimed in the '125 patent, like the SNES, is one designed for use with a television (a raster scanned display device). *See* id. para. 40. Pelovitz also states that "[p]lacing the picture data, which is stored in bits, onto the raster display is mapping bits because the bits directly determine the light or color of each spot on the raster. The SNES, as in the '125 patent, sequentially maps bits onto the raster of the TV." Id. para.para. 42-43.

As to element [h], Pelovitz simply concludes that the SNES incorporates the claimed "plurality of gating means." *See* id. para.para. 63-64.

c. Joel Snyder for GE

Joel Snyder ("Snyder") has been an electrical engineer practicing in the field of computer engineering for more than 40 years. *See* Snyder Decl. para. 1. Currently, he is a Senior Industry Professor at Polytechnic University, where he has taught courses on, *inter alia,* computers, microprocessors, switching and automata theory. *See* id. para. 2. He has been retained by GE to examine the '125 patent and to provide information regarding the state and terminology of the art in 1976. *See* id. para. 5. In preparing his declaration, Snyder reviewed the '125 patent, its file history and the documentation relating to the microprocessor used in the preferred embodiment of the '125 patent, known as "COSMAC." *See* id. para. 6.

Snyder's testimony is most relevant to whether the '125 patent is valid and is not addressed to the issue of infringement. Indeed, Snyder has not reviewed the SNES or other Nintendo products. While Nintendo has withdrawn its invalidity argument, parts of Snyder's testimony pertain to how the preferred embodiment of the '125 patent operates and what the patent claims. Not surprisingly, Snyder's conclusions are generally identical to Pelovitz's. The Court therefore deems unnecessary a detailed summary of Snyder's testimony. Briefly, Snyder asserts the following: (1) the '125 patent utilizes the DMA data transfer technique, a process by which data is transferred from one location to another within a computer system without intervention of the CPU, *see* id. para.para. 11, 24, 29-30; (2) the '125 patent displays images by "mapping bits," which refers to the pixel by pixel and line by line map of picture data necessary to drive a raster scan display

device, *see* id. para.para. 18-20, 23; and (3) the '125 patent's "gating means" has several purposes, including line repetition, and may be constructed interchangeably with AND gates or tri-state buffers, *see* id. para.para. 14-16, 40-49.

B. Discussion

Nintendo maintains that its SNES system neither literally infringes Claim 1 of the '125 patent nor infringes Claim 1 of the '125 patent under the doctrine of equivalents.

1. Literal Infringement

[24] For Nintendo to succeed on its motion, it must show that the SNES lacks at least one limitation of Claim 1. Claim 1 of the '125 patent is written in means-plus-function format. Thus, under 35 U.S.C. s. 112(6), Claim 1 must be construed to cover the corresponding structure described in the specification and equivalents thereof. *See supra* s. II.B.1.a (quoting language from s. 112(6)).

a. Data Transfer Technique

The two questions underlying the determination of whether Nintendo's motion should be granted with respect to the data transfer technique are: (1) whether the '125 patent requires the specific DMA circuitry disclosed in the specification; and (2) if not, whether the conventional definition of DMA excludes dedicated hardware circuitry that does not utilize the CPU data bus. If either answer is yes, the Court must conclude that the dedicated hardware circuitry in the SNES is fundamentally different from the DMA circuitry required by the '125 patent.

[25] As to the first question, Nintendo asserts that, under s. 112(6), the references to DMA in the preamble and elements [e] and [g] implicate the structure of the circuitry disclosed in the specification for transferring data. Thus, Nintendo maintains, the '125 patent is limited to DMA circuitry that shares the CPU data bus, as disclosed in the specification. GE disagrees, arguing that the references to DMA are not part of the means and therefore are not limited by the structure disclosed in the specification. While GE agrees that the '125 requires a DMA process, GE posits that the DMA process cannot be limited in structure by that disclosed in the specification. *See* GE's Br. in Opp. at 25-28.

Elements [e] and [g] of Claim 1 respectively claim "first decoder means ... for supplying direct memory access request to said computer" and "means for storing data signals ... when said computer responds to a direct memory access request." *See* Mayer Cert. Ex. A at col. 8, lines 10-12 and 16-19. Similarly, the preamble describes a system involving a computer that is "responsive to a direct memory access request." *See* id. Ex. A at col. 7, lines 56-57. Neither of the elements nor the preamble include DMA as part of the means. Nintendo nevertheless argues that s. 112(6) should apply to the DMA references, asserting that the circuitry which actually carries out the DMA transfer process cannot be disassociated from the means for requesting and responding to the DMA transfer. *See* Nintendo's Reply Br. at 6-7. The Court disagrees. That "DMA is an integral part of the functioning of the decoder and storing/shifting means recited in the elements," as Nintendo asserts, does not render the DMA requests and responses referred to in elements [e] and [g] subject to construction under section 112(6); DMA is simply not part of the claimed means. Thus, the Court holds that the '125 patent's DMA requirement is not subject to construction under s. 112(6) and the DMA transfers referred to in the above elements and preamble are not limited to the corresponding circuitry described in the patent. Nintendo therefore cannot escape the allegation of infringement by arguing under s. 112(6) that the '125 patent requires the specific DMA circuitry disclosed in the patent.

[26] Having answered the first question in the negative, the Court must pass on the second question-whether the conventional definition of DMA excludes dedicated hardware circuitry that does not utilize the CPU data bus. The Court holds that it does; the DMA technique is distinctly different from the dedicated

hardware technique. In so concluding, the Court has considered the specification and certain extrinsic evidence included in the record. The claim language and file history provide little meaning to the term.

The '125 patent indisputably requires a DMA process. A defining characteristic of the DMA process evidenced by both the specification and the extrinsic evidence is diminished processing time available to the CPU. *See* Mayer Cert. Ex. A at col. 3, lines 58-60 ("the processor time during display periods is necessarily devoted solely to display") and Ex. D at 137. In the latter cited reference, the inventor of the '125 patent, Weisbecker, stated that during Step B, "the contents of the refresh memory have to be transferred to the external circuitry through a direct memory access (DMA) facility. The amount of data transferred in this approach will strain or even break down the DMA process and leave little or no processing time for the CPU." *See* id. Ex. D at 137. This lack of available processing time results from the fact that the DMA circuitry uses the CPU data bus. *See* id. para. 60(b).

By contrast, the SNES is indisputably not burdened with this problem because its dedicated hardware does not use the CPU data bus. The SNES's dedicated hardware approach renders the CPU free to perform other functions even while the dedicated hardware performs Step B. *See* id. para. 60(c). The use of dedicated hardware is integral to the SNES's ability to produce complex video images, an ability that the '125 lacks due to its DMA approach.

Based on the record before it, the Court concludes that the conventional concept of the DMA technique, as used in the '125 patent, does not include the use of dedicated hardware that utilizes its own data bus, thereby leaving the CPU available to perform other tasks during Step B data transfers. FN57 The distinction between the DMA technique and the dedicated hardware technique was starkly recognized in the 1970s by an RCA engineer: "There are two popular techniques for display refresh, DMA and dedicated-hardware controlled." *See* id. Ex. C at 18.

FN57. In light of the myriad of tasks the SNES' CPU can still perform, the Court's conclusion that the two techniques differ is not altered by the fact that the SNES' CPU cannot load additional images into the VRAM during Step B.

Therefore, because the preamble and elements [e] and [g] of Claim 1 of the '125 patent require a DMA process for transferring data in Step B and because the SNES utilizes a distinct dedicated hardware process in Step B, the Court holds that the SNES does not infringe Claim 1 of the '125 patent. Summary judgment on this ground in favor of Nintendo is therefore appropriate.

b. Refresh Technique

[27] The threshold question to the determination of whether the Court will grant Nintendo's motion with respect to the refresh technique is whether the '125 patent claims a bit map display system.

Nintendo's assertion that the '125 patent claims a bit map system is rooted in the "mapping bits" language of the preamble to Claim 1. Despite GE's argument to the contrary, the Court finds that the preamble is incorporated by reference throughout the body of the claim and, thus, constitutes a limitation of the claim. *See, e.g.,* Bell Communications Research, Inc. v. Vitalink Communications Corp., 55 F.3d 615, 620-21 (Fed.Cir.1995). As the Federal Circuit has stated, "when the claim drafter chooses to use *both* the preamble and the body to define the subject matter of the claimed invention, the invention so defined, and not some other, is the one the patent protects." Id. at 620. In Claim 1 of the '125 patent, the various elements make significant reference to the items defined in the preamble. For example, the antecedent basis for the terms "said computer," "said data bus," and "said data" in claim elements [e] and [g] are found in the preamble of the claim. The preamble is necessary to give meaning to the claim elements and, therefore, must be given

the effect of a limitation. *See* id. at 620-21 (quoting Kropa v. Robie, 187 F.2d 150, 152 (C.C.P.A.1951)). Once deemed a limitation, the Court construes the preamble like all other claim language. *See id*. at 620-21 ("Preamble construction thus presents no deeper mystery than the broader task of claim construction, of which it is but a part.").

Nevertheless, while concluding that the preamble constitutes a claim limitation, the Court rejects Nintendo's argument that the "mapping bits" language is part of a means, such that s. 112(6) would apply. Similarly, the Court finds that the means in elements [e] and [g] have nothing to do with a "bit map display system." As such, s. 112(6) is inapplicable, and the Court must construe "mapping bits" as any other claim limitation. *See* Markman, 52 F.3d at 979-80.

The preamble claims "[a] system for displaying ... by mapping bits ... onto a raster." GE contends that "the 'mapping bits' language merely specifies that the invention is intended to be used with raster scan displays." GE's Br. in Opp. at 30. The specification and, more forcefully, the prosecution history contradict GE's assertion. Thus, the Court disagrees with GE that the '125 patent does not require a bit map display system.

The '125 patent specification supports this conclusion. The specification provides that "[t]he video display is accomplished by mapping the memory bits devoted to the display onto a standard television raster." Mayer Cert. Ex. A at col. 2, lines 23-26; *see also* id. Ex. A at col. 2, line 29 to 48. The description of the refresh technique in the specification further speaks of bits that are "devoted" to the display, that "represent[ ] a point on the raster," and that "correspond" to spots on the screen. The specification thus lends to the conclusion that the '125 patent requires a complete screen bit-mapped memory where bits in memory relate to spots on the television screen on a one-to-one basis.

Any ambiguity left by the specification is filled in by the prosecution history. During the prosecution of the '125 patent, the RCA attorney distinguished the '125 patent from a prior art reference that used a character generation display system. In so doing, the attorney stated the following:

[The '125 patent] synchronizes the operation of a computer's direct memory access with the display device and displays the data as taken from the memory onto the display. On the other hand, the system of Reference A ... reads a character from memory in the form of binary bits, decodes the character into a matrix of dot elements, and then displays the dot matrix to provide the configuration of the character. The circuit of Reference A is thereby restricted only to characters which are coded into stored binary values and capable of being generated by the character generator, whereas the system of the ['125 patent] can display any desired configuration of dots.

Bergin Cert. Ex. B at 41-42. While GE asserts that this comment was made in the context of distinguishing the data transfer processes used by the two inventions, its significance to the present issue cannot be ignored. In that statement, the RCA attorney acknowledged the difference between the '125 patent and a character generation display system. Faced with the character generation system utilized in the SNES, GE cannot now retract that statement or otherwise argue against its meaning. *See* Alpex Computer Corp. v. Nintendo Co. Ltd., 102 F.3d 1214, 1220-21 (Fed.Cir.1996), *cert. denied,* 521 U.S. 1104, 117 S.Ct. 2480, 138 L.Ed.2d 989 (1997) ("Prosecution history is relevant not only for purposes of prosecution history estoppel but also for construing the meaning and scope of the claims.").

Based on the above, the Court concludes that the '125 patent requires a bit-map display system.FN58 Because the SNES uses a character generation system, a distinctly different refresh technique, the Court holds that the SNES does not literally infringe Claim 1 of the '125 patent with respect to the '125 patent's requirement of a bit-map display system. Summary judgment in favor of Nintendo is therefore appropriate on this basis as well.

FN58. GE insists that such a conclusion is not credible because the term "bit-mapping" is not found in the patent or prosecution history. *See* GE's Br. in Opp. at 32. The Court does not view this fact as prohibitive of the above conclusion. Indeed, in *Alpex,* neither the patent nor its file history used the term "bit mapping." Nevertheless, the Federal Circuit found the patent at issue to require a bit-map system because the patent described a system that utilized a display memory with storage locations corresponding to each of the dots on the television screen. *See* Alpex, 102 F.3d at 1216. The Court similarly concludes here.

c. Gating Means

[28] Element [h] of Claim 1 requires a "plurality of gating means, responsive to a command signal, for coupling the output signals from the line counter means to the data bus means." Pursuant to s. 112(6), this means-plus-function element must be construed to cover only the corresponding structure disclosed in the '125 patent specification and equivalents thereof. *See* 35 U.S.C. s. 112(6) (1984). Section 112(6) "means exactly what it says: To determine whether a claim limitation is met literally, where expressed as a means for performing a stated function, the court must compare the accused structure *with the disclosed structure,* and must find equivalent *structure* as well as *identity* of claimed *function* for that structure." Pennwalt Corp. v. Durand-Wayland, Inc., 833 F.2d 931, 934 (Fed.Cir.1987), *cert. denied,* 485 U.S. 961, 108 S.Ct. 1226, 99 L.Ed.2d 426 (1988) (emphasis in original).

The only structure in the patent corresponding to the "gating means" is the specific circuit arrangement set out in figure 1 of the patent in which the five highest stages of the line counter are connected to the data bus by a set of AND gates. *See* Mayer Cert. Ex. A fig. 1 (attached as App. 4) and col. 7, lines 4-14. Through this configuration, the '125 display system is able to repeat the same picture information on eight consecutive display lines. This helps to clarify the crude image that the '125 patent produces and is the only purpose of the "gating means" discussed in the patent. *See* GE's Br. in Opp. at 12 (acknowledging use of gating means for line repetition). Indeed, in the absence of a structure that coupled less than all of the gates, the '125 patent would be unable to repeat picture information on consecutive lines. No other purpose for the gating means is disclosed in the patent or its file history, although GE baldly asserts that the disclosed structure "allows the CPU to use the line count values in a number of ways." Id.

The SNES also couples the line counter to the data bus. Unlike the structure disclosed in the '125 patent, however, the SNES couples *all* of the stages of the line counter to the data bus.FN59 This structure cannot practically be used for line repetition because the CPU determines the horizontal line currently being displayed. This allows the SNES to create effects such as scrolling the image on the display from left to right and computing the exact location on the screen where a random event (*e.g.,* the firing of a light gun) has occurred. The SNES, unlike the disclosed structure of the '125 patent, does not have a plurality of gates that couples only a portion of a line counter to a data bus for any purpose. Thus, the SNES lacks the requisite equivalent structure of the '125 patent. *See* Pennwalt, 833 F.2d at 934.

FN59. GE's assertion that "Nintendo's Mayer has admitted that not all of the outputs of Nintendo's line counter are coupled to the data bus" is incorrect. *See* GE's Br. in Opp. at 21, n. 13. The SNES has a nine-bit counter that is read in two stages-eight bits and then one bit. As Nintendo explains, this is necessary because the data bus in the SNES is capable of carrying only eight bits of information at a time. *See* Nintendo's Reply Br. at 4.

Based on the above distinction between the disclosed structure of the gating means in the '125 patent, which corresponds to the means of element [h] of Claim 1, and the structure of the gating means in the SNES, the Court concludes that the SNES does not literally infringe element [h] of Claim 1. Summary Judgment in favor of Nintendo is thus appropriate on this third basis.

2. Infringement Under the Doctrine of Equivalents

[29] In addition to a literal infringement analysis, the Court must also consider whether the SNES infringes Claim 1 of the '125 patent under the doctrine of equivalents.

First, as to the data transfer technique, the Court finds the SNES' dedicated hardware system to be fundamentally different from the DMA approach claimed in the '125 patent. The SNES incorporates added components (*i.e.,* PPUs and VRAM), which are not found in the '125 patent. Moreover, the SNES' method of data transfer facilitates the creation of complex, high quality images, whereas the '125 patent produces simple images. As stated by Nintendo, "while the display generated by the '125 display system is a simple black and white display with only 64 spots per horizontal line and only 128 horizontal lines per frame ... [the SNES] generate[s] displays consisting of 240 or more horizontal lines, each of which consists of 256 or more spots. Each spot can be any one of 32 or more colors." Nintendo's Br. at 31. Any argument that the data transfer techniques in the '125 patent and SNES are substantially similar in structure, function and result must be rejected.

Second, the Court holds that the SNES' character generation system is structurally distinct from the '125 patent's bit-map system.FN60 *See* Mayer Cert. para.para. 100-02. Most notably, as recognized by RCA in the prosecution history and as evinced by the actual operation of the SNES' character generation system, the SNES cannot alter a single dot of data in memory. The SNES, instead, stores pre-constructed character stamps in its memory and displays these stamps on the television screen. *See* id. para. 100. This fundamental distinction is dispositive of the issue of equivalence. *See* Alpex, 102 F.3d at 1220, 1222-24 (distinguishing bit-map systems from character generation systems).

FN60. This fact was plainly acknowledged by RCA in the 1970s: "The function of video generation usually follows one of two techniques, bit mapped or character generation." Mayer Cert. para. 84 and Ex. C at 18; *see also id*. Ex. D at 135-37.

Finally, the Court finds substantial difference between the gating means in the '125 patent and that in the SNES. Because in the SNES all of the stages of the line counter are coupled to the data bus, the SNES has no way to repeat lines on the display. This contrasts the primary, if not the only, function of the gating means structure in the '125 patent. As compared to the '125 patent's gating structure, the SNES does not "perform substantially the same function in substantially the same way to achieve substantially the same overall result as the claimed invention." *See* Graver Tank & Mfg. Co., 339 U.S. at 608, 70 S.Ct. at 856.

For all these reasons, the Court holds that the SNES does not infringe Claim 1 of the '125 patent under the doctrine of equivalents. As no genuine issue of material fact exists, summary judgment on this ground is likewise appropriate.

V. CONCLUSION

For the reasons set out above, the Court will (1) grant Nintendo's Motion for Summary Judgment of Non-Infringement and Invalidity of Claims 12-14 of the '899 patent; (2) grant Nintendo's Motion for Summary Judgment of Non-Infringement of Claims 1, 3, 4, 5 and 13 of the '659 patent; and (3) grant Nintendo's Motion for Summary Judgment of Non-Infringement of Claim 1 of the '125 patent.

An appropriate Order is attached.

ORDER

In accordance with the Court's Opinion filed herewith,

It is on this 6th day of October, 1997

ORDERED that Nintendo Company Ltd. and Nintendo of America, Inc.'s (collectively, "Nintendo") Motion for Summary Judgment of Non-Infringement and Invalidity of Claims 12-14 of United States Patent No. 4,097,899 is granted; and it is further

ORDERED that Nintendo's Motion for Summary Judgment of Non-Infringement of Claims 1, 3, 4, 5 and 13 of United States Patent No. 4,169,659 is granted; and it is further

ORDERED that Nintendo's Motion for Summary Judgment of Non-Infringement of Claim 1 of United States Patent No. 4,270,125 is granted.

APPENDIX 1

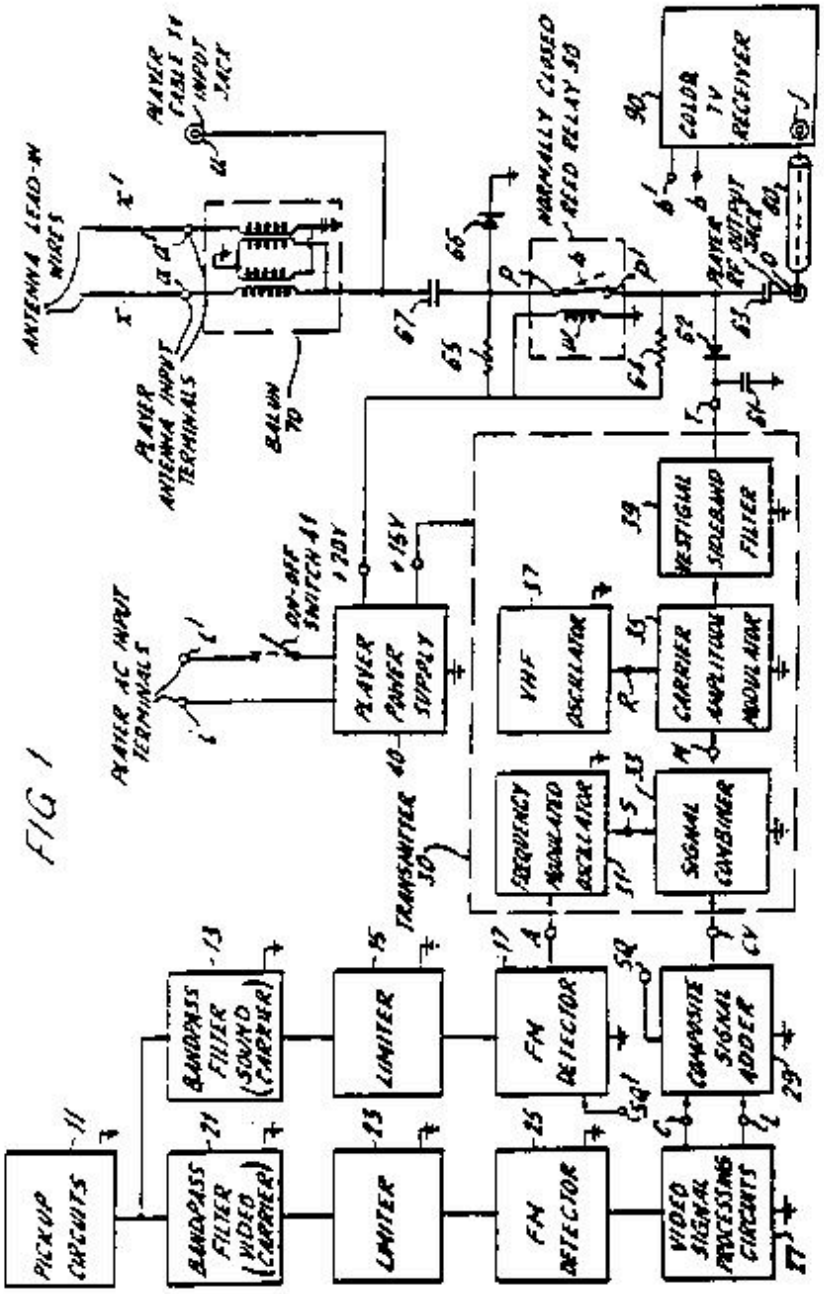
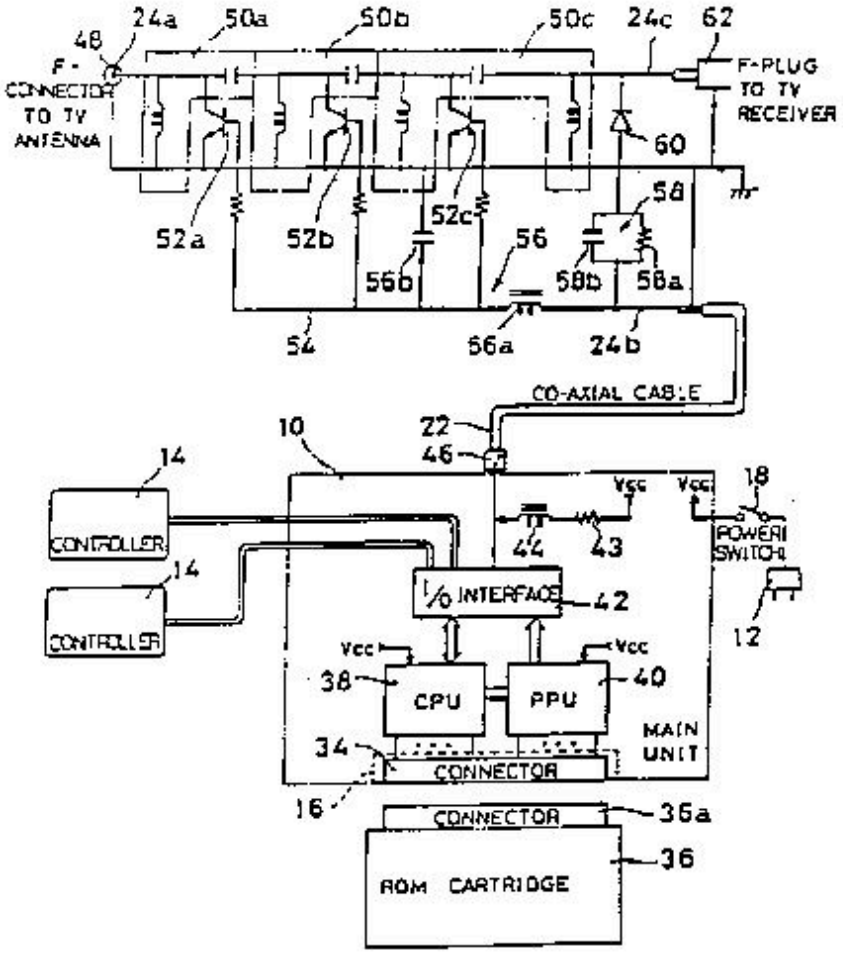


FIG 1

APPENDIX 2

FIG. 2



APPENDIX 3

Claim Chart for U.S. Patent No. 4,097,899 and
Sharp Japanese Patent Application 50-111922 (Sharp II)

Patent Claim 12	Invalidity Analysis
12. Video record player apparatus comprising:	Sharp II discloses a video recorder-player. The term "magnetic recording/playback device" is used throughout the document. It is clear that video signals can be played back from the reference to the "video-audio signal." (Page 2, col. 1, lines 20-30; page 3, col. 2, lines 22-26).
[a] a player RF signal input terminal; Corresponding Structure in '899 Patent Player antenna input terminals a a' or player cable TV input jack u. (Col. 4, lines 4-5)	Sharp II discloses input terminals A-A which are connected to a VHF TV antenna. (Page 2, col. 2, lines 26-27; page 3, col. 1, lines 38-39).
[b] a player RF signal output terminal; Corresponding Structure in '899 Patent Output jack O. (Col. 4, lines 34-37).	Sharp II discloses an "output terminal B" that goes to a television receiver. (Page 3, col. 1, line 13).

Patent Claim 12

[c] **a player power supply developing supply potentials when selectively enabled;**

Corresponding Structure in '899 Patent

Player power supply 40, which develops a +20V potential and a +15V potential when on-off switch 41 is switched to the "on" condition. (Col. 3, lines 49-60).

Invalidity Analysis

A power supply provides power to the magnetic recording playback device in Sharp II and supplies +B power to relay coil L when power to Sharp II is on. (Page 3, col. 1, lines 5-8 and col. 2, lines 27-29). In addition, +B supplies power to the components D1 to D3, VCD1 and VCD2 through relay switch S1. (Figure 2 and page 3, col. 2, lines 29-35).

Patent Claim 12

(d) means, rendered operative in response to supply potential development by said power supply, for forming a player output signal inclusive of picture carrier frequency oscillations and sound carrier frequency oscillations;

Corresponding Structure in '899 Patent

Transmitter 30, which is powered by the +15V potential from the player power supply. (Col. 3, lines 55-59)

Invalidity Analysis

Same Function

The same function of forming a player output signal is performed in Sharp II by the RF converter 5. (Page 3, col. 2, lines 22-29).

Equivalent Structure

The structure for performing this function in Sharp II (RF converter 5) is equivalent to the structure disclosed in the '899 patent (transmitter 30).

Figure 1 in Sharp II depicts an RF switch 2 that selects the signal from either the antenna 3 or the RF converter 5 and routes the selected signal to the television receiver 1. (Page 2, col. 1, lines 23-42).

When power is on in Sharp II, the RF converter generates RF signals from the magnetic recording/playback device signals. In particular, video and audio signals from the magnetic recording/playback device are sent to the RF converter where they are converted to VHF band TV signals. (Page 3, col. 2, lines 22-29). Because these VHF signals can be viewed and heard on an ordinary television receiver, (Page 2, col. 1, lines 23-31), they necessarily include picture carrier frequency oscillations and sound carrier frequency oscillations.

Patent Claim 12

[e] means, responsive to supply potential development by said player power supply, for establishing a first signal path[*] between said output signal forming means and said player RF signal output terminal; said first signal path being disrupted in the absence of supply potential development by said player power supply; and

---

* In the patent the signal path between the player and the TV is referred to inconsistently. In column 3 it is called the "second signal path" (lines 41, 49 and 58), but it is called the "first signal path" in claim 12.

Corresponding Structure in '899 Patent

Diode 62.

When the +20V potential is present, a current flows from the power supply, through resistor 64 and diode 62, which causes diode 62 to turn "on" (i.e. conduct). This establishes a path between the player output signal at terminal T and terminal O. (Col. 3, line 65 - Col. 4, line 4).

When the +20 V potential is absent, diode 62 is off, and the signal path is disrupted (Col. 4, lines 18-27).

Invalidity Analysis

Same Function

The same functions of establishing and disrupting are performed in Sharp II by relay switch S2.

As shown in Figure 2, when the power in Sharp II is on, S2 establishes a signal path between the player's RF converter input Terminal C and the output terminal B to the TV set. When power is off, S2 disrupts this path. This function is performed automatically as power is turned on and off. (Page 3, col. 1, line 5 to col. 2, line 41; page 4, col. 2, lines 30-40).

Equivalent Structure

The structure for performing these functions in Sharp II (relay switch S2) is equivalent to the structure disclosed in the '899 patent (diode 62).

Diode 62 in the '899 patent and relay switch S2 in Sharp II are both used in the series path between the local RF source and the TV set to switch RF signals. In both cases, the signal path passes through the switching element itself.

When power to the Sharp II unit is on, power is supplied to the relay coil L. (Page 3, col. 1, lines 5-10). When power is supplied to the relay coil, relay switch S2 switches to its lower position, establishing the signal path from the RF converter input C to the TV output B (passing through capacitor C6). (Page 3, col. 2, lines 27-41). This is equivalent to diode 62 in the '899 patent which is on (i.e. conducting) whenever power is on, thereby establishing the first signal path.

Patent Claim 12

Invalidity Analysis

Figure 2 depicts the Sharp II unit when the power supply is off. In this state, the signal path between the VTR RF converter input C and the TV output B is disrupted by the high series impedance introduced by the open contacts of relay switch S2. (Page 3, col. 1, lines 20-33).

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Patent Claim 12

[f] means, responsive to the absence of supply potential development by said player power supply, for establishing a second signal path[*] between said player RF signal input terminal and said player RF signal output terminal; said second signal path being disrupted in the presence of supply potential development by said player power supply.

* The "second signal path" of claim 12 -- the antenna/TV path -- is called the "first signal path" at column 1, lines 36, 47 and 59.

Corresponding Structure in '899 Patent

Relay 50.

When the +20 V potential is absent, power is not applied to relay 50's coil. This coil is therefore not energized so the contacts remain in their normal, closed, position. Therefore, the signal at antenna terminals a' or cable jack u is linked to the output jack O (Col. 4, lines 18-23).

When the +20V potential is present, power is applied to relay 50's coil. This energizes the coil, opening the contacts and

Invalidity Analysis

Same Function

The same function is performed in Sharp II by S2.

When the power is off in Sharp II, relay switch S2 establishes a signal path between the upper antenna input terminal A and the TV output terminal B. When power is on, the switch disrupts this path. This function is performed automatically as power is turned on and off. (Page 3, col. 1, lines 5-33 and col. 2, lines 22-41).

Same Structure

Figure 2 depicts the Sharp II unit when the power supply is off, with relay switch S2 in its upper position. In this state, a signal path is established between the upper antenna input A and the TV output B. This path passes through S2 and a group of capacitors and variable capacitance diodes which pass the relevant RF frequencies. (Page 3, col. 1, line 20 to col. 2, line 21 and Figure 2).

When power is turned on, relay switch S2 switches to its lower position, which disrupts the signal path between the antenna input A and the TV output B. (Page 3, col. 2, lines 22-41).

(In addition to the structure corresponding to subparagraph f of claim 12, Sharp II also includes additional circuitry to provide extra isolation between the VTR's RF converter output and the antenna. When the relay contacts are in the power-on position, voltage +B is supplied through relay switch S1 to the top ends of resistors R1, R4, and R7. This provides a forward bias to diodes D1 to D3, causing them to conduct. When diodes D1 to D3 conduct, the signal arriving from the antenna is shunted to ground

Patent Claim 12	Invalidity Analysis
disrupting the signal path. (Col. 3, line 62 - Col. 4, line 10).	through diodes D1 to D3. In addition, signals from the RF converter that leak past the opened relay contacts will also be shunted to ground through D1 to D3 before reaching the antenna. (Page 3, col. 2, line 22 to page 4, col. 2, line 12). Thus, diodes D1 to D3 perform the same function as, and are identical in structure to, diode 66 in the '899 patent. (Extra isolation is provided by the variable capacitance diodes VCD1 and VCD2 when power to the Sharp II unit is on. When the relay contacts are in the power-on position, voltage +B is supplied through relay switch S1 to the top ends of resistors R2 and R5. This voltage provides a reverse bias to the variable capacitance diodes VCD1 and VCD2. When these variable capacitance diodes are reverse biased, their capacitance decreases, thereby increasing the impedance of the signal path through the variable capacitance diodes and providing an additional measure of isolation at the relevant frequencies. (Page 3, col. 2, line 29 to page 4, col. 2, line 12)).

*580

Patent Claim 13	Invalidity Analysis
13. A system for utilizing the video record player apparatus of claim 12, said system also including:	See discussion for claim 12, above.
[a] a television receiver having an RF signal input terminal;	Sharp II discloses a television receiver. (Page 1, col. 2, line 47; page 2, col. 1, line 30).
Corresponding Structure in '899 Patent Color television receiver 90 includes an RF input jack "j" and balanced input terminals b, b'. (Col. 4, lines 37-45 and Figure 1).	An RF signal input terminal on the television receiver is inherent in Sharp II because RF signals are supplied to the television receiver via the output terminal B, and the output terminal B is designed to be connected to a television receiver. (Page 3, col. 1, lines 13-14 and col. 2, lines 36-41).
[b] an external RF signal source;	VHF antenna 3 provides a broadcast signal to the Sharp II device. (Page 3, col. 1, lines 37-39).
Corresponding Structure in '899 Patent A broadcast receiving antenna. (Col. 1, lines 33-34).	

Patent Claim 13	Invalidity Analysis
[c] **means for coupling said player RF signal output terminal to said television receiver RF signal input terminal; and** Corresponding Structure in '899 Patent A suitable shielded cable 80 linking jacks O and j. (Col. 4, line 41).	These coupling means are inherent in Sharp II because output terminal B is designed to be connected to a television receiver. (Page 3, col. 1, lines 13-14). While no particular structure for coupling is shown, various means for coupling, including the use of coaxial cable and the appropriate connectors, are commonplace in the art of RF circuit design.
[d] **means for coupling the output of said external RF signal source to said player RF signal input terminal;** Corresponding Structure in '899 Patent The connection between balanced antenna lead in wires x, x' and the player's antenna input terminals a, a'. (Col. 4, lines 32-34).	These coupling means are inherent in Sharp II because input terminals A-A are designed to be connected to a VHF antenna. (Page 2, col. 2, lines 26-27). While no particular structure for coupling is shown, various means for coupling, including the use of coaxial cable and the appropriate connectors, are commonplace in the art of RF circuit design.

Patent Claim 13

[e] **whereby said television receiver receives the output of said external RF signal source during player power supply disabling; whereas said television receiver receives said player output signal, to the exclusion of the output of said external RF signal source, during player power supply enabling.**

Corresponding Structure in '899 Patent

When power supply 40 is disabled, the signal from the antenna arriving via lead-in wires x,x' is linked to the player's output jack (and to the television receiver), because relay 50 is closed and diode 62 is off. (Col. 4, lines 18-27)

When power supply 40 is enabled, the signal from the transmitter 30 is linked to the player's output jack (and to the television receiver), because relay 50 is open and diode 62 is on. (Col. 3, line 65 - Col. 4, line 6).

Invalidity Analysis

When the power supply is disabled in Sharp II (i.e., when power is off), the relay coil L is not energized and relay switch S2 passes the signals from the external RF signal source (i.e., VHF antenna 3) to the output terminal, so the antenna signals can be received by the television receiver. (Page 3, col. 1, line 20 to col. 2, line 21).

When the power supply is enabled (i.e., when power is on), the relay coil is energized and relay switch S2 passes the video player output signals from the RF converter 5 to the output terminal, so the video player output signals can be received by the television receiver. S2 also disrupts the signal path between the antenna and the television receiver, so that the signal from the antenna is not received by the television receiver. (Page 3, col. 2, lines 22-41).

*583

Patent Claim 14	Invalidity Analysis
14. Apparatus in accordance with claim 13,	See discussion for claim 13, above
[a] **wherein said source output coupling means comprises an antenna coupling element,**	These coupling means are inherent in Sharp II, as explained above, because the input terminals A-A are designed to be connected with the VHF antenna. (Page 2, col. 2, lines 26-27).
Corresponding Structure in '899 Patent The connection between balanced antenna lead in wires x, x' and the player's antenna input terminals a, a'. (Col. 4, lines 32 34)	While no particular coupling element is explicitly shown, various coupling elements, including coaxial cable and the appropriate connectors, are commonplace in the art of RF circuit design.
[b] **said antenna coupling element being isolated from player RF signal output terminal and said player output signal forming means during player power supply enabling by the disruption of said second signal path.**	When the power supply is enabled (i.e., when power is on) any antenna coupling element would be isolated from output terminal B and the output signal forming means (i.e., the RF converter). This isolation is provided by relay switch S2 when S2 disrupts the signal path to the antenna. (Figure 2 and page 3, col 2, lines 22 to 41).
Corresponding Structure in '899 Patent The coupling element between balanced antenna lead in wires x, x' and the player's antenna input terminals a, a' would be isolated from the player output by the relay 50 when the second signal path is disrupted. (Col. 3, line 65 - Col. 4, line 5 and Col. 4, lines 32-34).	

P30/5A515792/jc

APPENDIX 4

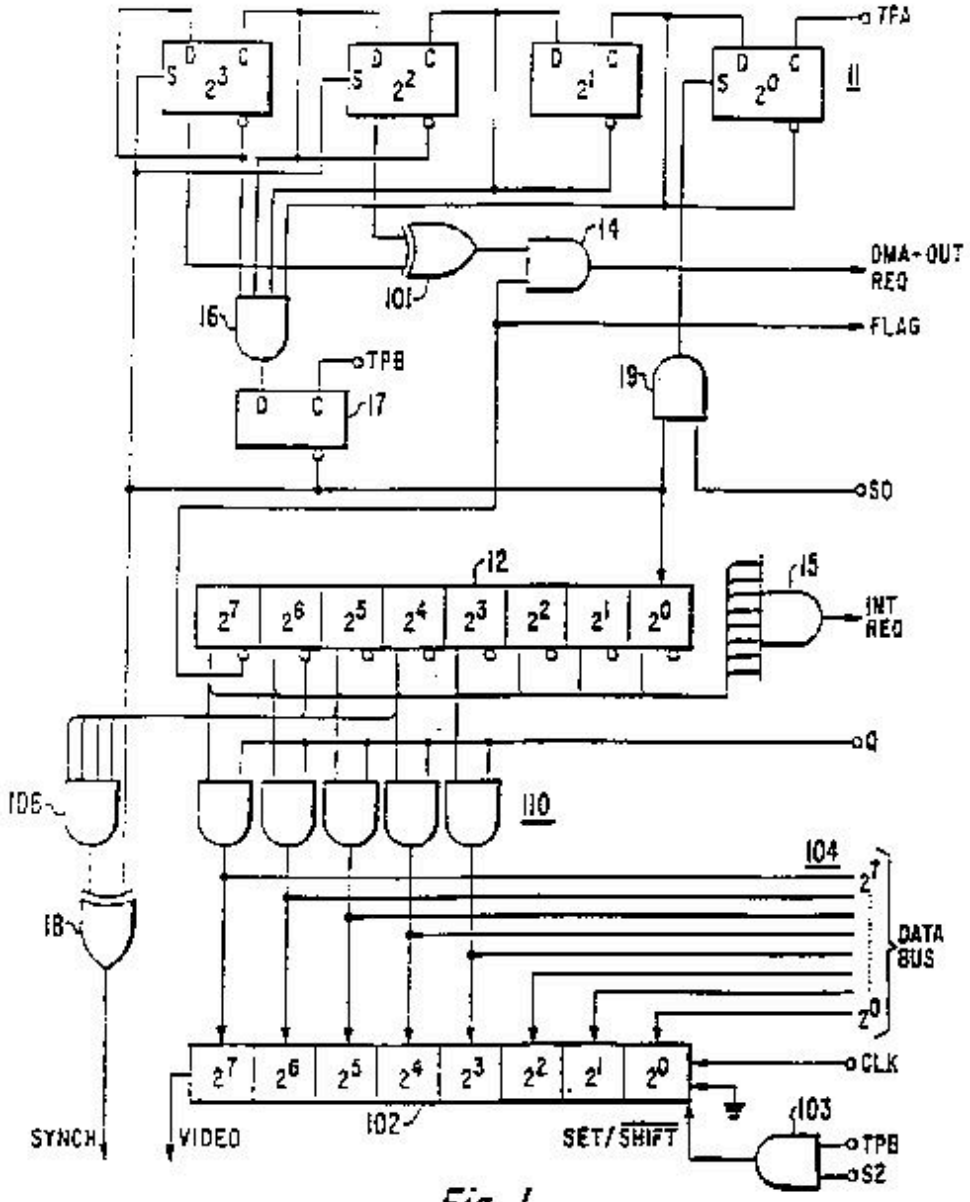

Fig. 1.